Organic Thin Film Transistors: Integration Challenges

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I, James Stott confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

Abstract

This thesis considers some of the requirements and challenges in the field of organic thin film transistors (OTFTs), from the standpoint of large scale integration using low temperature plastic compatible processes.

A combination of processes and materials for use in the fabrication of OTFTs is developed, yielding device performance comparable with the state of the art for bottom-contact, bottom-gate, organic small molecule thin film transistors. High quality silicon nitride (SiN_x) gate dielectric material is developed using plasma enhanced chemical vapour deposition (PECVD) at a low temperature (150 °C) compatible with plastic substrates. A variety of high quality films are developed, allowing an investigation into the impact of changes in SiN_x composition on OTFT performance.

Surface modification strategies on SiN_x substrates are considered, leading to almost an order of magnitude enhancement in OTFT performance, suggesting a suitable device architecture for large scale integration, and exploitation of novel organic material properties.

We then examine organic semiconductor nanowire devices, which have begun to emerge as a new and exciting class of device in recent years.

This work explores the possibilities of combining traditional thin film transistor fabrication techniques with novel organic nanowires and examines the resultant transistor device behaviour. Two-dimensional arrays of nanowire devices are analysed, demonstrating the suitability of devices for large area applications.

The combination of a large area and plastic compatible, low temperature dielectric with well known organic semiconductors in thin film devices suggests that the integration of novel organic nanowires could provide an exciting performance enhancement over traditional OTFT devices.

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Nomenclature

a-Si	amorphous silicon.
AFM	atomic force microscopy.
AMOLED	active matrix organic light emitting diode.
BCBG	bottom-contact bottom-gate.
BCTG	bottom-contact top-gate.
C-V	capacitance-voltage characteristics.
CMOS	complimentary metal oxide semiconductor.
Cu	copper.
CuPc	copper phthalocyanine.
DI	de-ionised (water).
EA	electron affinity.
EF	Fermi energy level.
F_{16}CuPc	hexadecafluoro-copper phthalocyanine.
FTIR	fourrier transform infrared spectroscopy.
H_2	hydrogen.
He	helium.
HMDS	hexamethyldisilazane.
HOMO	highest occupied molecular orbital.
I-V	current-voltage characteristics.
IC	integrated circuit.
IP	ionization potential.
LCD	liquid crystal display.

LED	light emitting diode.
LUMO	lowest unoccupied molecular orbital.
MOSFET	metal oxide semiconductor field effect transistor.
nc-Si	nano-crystalline silicon.
NH_3	ammonia.
NW	nanowire.
OMBD	organic molecular beam deposition.
OPV	organic photovoltaic.
OTFT	organic thin film transistor.
OTS	octadecyltrichlorosilane.
OVPD	organic vapour phase deposition.
PECVD	plasma enhanced chemical vapour deposition.
PHTS	phenethyltrichlorosilane.
RF	radio frequency.
RIE	reactive ion etching.
sccm	standard cubic centimetre per minute.
SEM	scanning electron microscopy.
Si	silicon.
SiH_4	silane.
SiN_x	silicon nitride.
SiO_2	silicon oxide.
TCBG	top-contact bottom-gate.
TCTG	top-contact top-gate.
TEM	tunelling electron microscopy.
TFT	thin film transistor.
UV	ultra-violet.
WF	work function.
XRD	X-ray diffraction.

Chapter 1

Introduction

1.1 Organic Large Area Electronics

Organic large area electronics is as field which has emerged in recent years to attract significant research attention and investment alike. As various technological and economic barriers are removed it is widely expected that organic electronics will spread further into the applications dominated thus far by inorganic thin film materials, and extend the reach of thin film electronics to products and devices previously impossible for various reasons.

Organic semiconductors themselves emerged in the mid-twentieth century, with early reports of electro-luminescence in organic crystals [7, 8] leading to the first organic light emitting diode (OLED) to be demonstrated in the late 1980s [9], soon to be followed by a similar report using polymer semiconductors [10]. Meanwhile, organic thin films were also being considered for use in transistors, with the first demonstration of an organic thin film transistor (OTFT) reported in 1983 [11].

Both classes of devices (OLED and OTFT) became more widespread through the 1990s, with great progress made in particular with OLEDs [12], which have now been adopted for use in many consumer electronic applications, with improved contrast and colour levels over liquid crystal display (LCD) alternatives in display applications. OTFTs, on the other hand have yet to be integrated into volume consumer products on the scale seen in OLEDs, owing largely to the

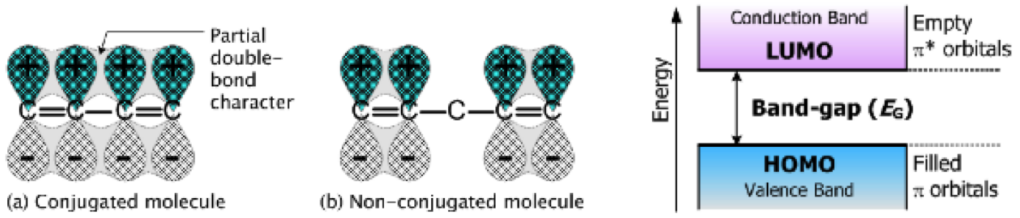
integration and stability challenges which have limited their competitiveness with existing technologies thus far.

OTFTs are however at last becoming close to exploitation in commercial products [13, 2] with the largest areas of exploitation initially likely to be active-matrix organic light emitting diode (AMOLED) displays and microelectronic circuits such as radio frequency identification (RFID) transponders, due to their requirements for large area, and low cost respectively. Crystalline silicon based metal oxide semiconductor field effect transistors (MOSFETs) remain the dominant device in mainstream semiconductor applications, with high speeds and stability, and low cost per device meaning they are unlikely to be unseated in the near future. The second most important device, in terms of commercial significance, is the hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT) [14], with displays making up by far the largest part of this market. However, the emergence of organic TFTs with comparable or improved operating characteristics [15] means that the promise of organic materials to replace a-Si:H is becoming a reality.

However, eventually, it is not just the display industry that stands to be revolutionised by OTFTs. The varied nature of organic semiconductors allows them to be considered for a great number of potential applications. While some materials, such a pentacene [16], can provide carrier mobilities similar to those observed in a-Si:H, it is applications requiring interfaces with organic materials systems, such as chemical and biological sensors [17] that stand to gain the most. The ability to integrate organic devices with various functions onto one substrate will enable the number of applications targetted to be dramatically increased, using, for example active matrix OTFTs to drive OLED displays, or high-performance OTFTs to perform readout of biological or chemical information from sensor arrays.

1.1.1 Charge Transport

Charge transport in organic molecules exists due to the molecular conjugation, the presence of alternate single and double bonds between adjacent carbon atoms, as illustrated by figure 1.1a. This phenomenon effectively releases one in four



(a) Conjugation in organic molecules

(b) Energy band structure in organic semiconductors

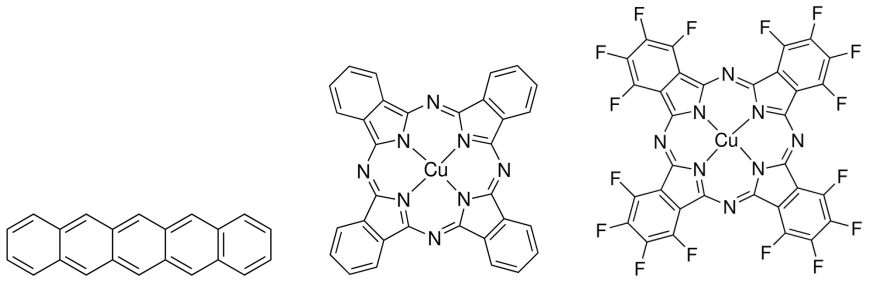
Figure 1.1: Conjugation and energy band structure of organic semiconductors [1].

electrons from the outer shell of each carbon atom, allowing them to become delocalised along the length of the conjugated system. Typically this can be from a few atoms (small molecules) to many tens or hundreds of atoms (polymers). While charge transport can be efficient along this length scale it is not the case between molecules, which are often bonded only weakly by van der Waals interactions, meaning delocalised wave functions do not spread through the entire volume of organic solid, but instead for a finite number of molecules.

The alternating double and single bonds of the conjugation system gives rise to bonding and anti-bonding states, which, due to no two states being allowed an identical energy level, form a band-like structure. The highest occupied molecular orbital (HOMO) is much like the valence band in inorganic semiconductors, consisting of bonding states which are filled with electrons, while the lowest unoccupied molecular orbital (LUMO) is similar in behaviour to the conduction band, consisting of empty states.

Highly crystalline forms of many small molecule organic semiconductors exist, but grain boundaries still present a significant barrier to efficient charge transport in these materials. In general, charge transport in organic materials is controlled by trapping in localised states [18, 19], with hopping from one molecule or grain to another under the influence of an applied electric field, a thermally activated process.

Typically, the dimensions of a practical thin film organic electronic device are significantly greater than the individual grain size, meaning that charge transport must be driven both intra- and inter-grain encountering multiple bonding



(a) Pentacene **(b)** CuPc **(c)** F_{16}CuPc

Figure 1.2: Chemical structure of pentacene, copper phthalocyanine and hexadecafluorocopper phthalocyanine.

configurations and effective barriers, or increased trap densities along the way.

Charge carrier mobilities observed in organic materials can vary significantly, not only between materials with differing degrees of conjugation or tendencies to form highly ordered mircrostructures, but also between different preparations of identical materials. Semiconducting polymers, with characteristic long chains weakly interacting with one another typically exhibit mobilities in the order of 10^{-6} to 10^{-3} cm^2/Vs [2]. Small molecule semiconductors, such as pentacene, can exhibit mobilities as high as 6 cm^2/Vs [20], when forming highly ordered polycrystalline films.

In particular, this work will focus on the contributions of two common small molecule organic semiconductors, pentacene and copper phthalocyanine.

1.1.2 Small Molecule Organic Semiconductors

1.1.2.1 Pentacene

As mentioned above, pentacene is a small molecule organic semiconductor (figure 1.2a) which has been used widely since the first report of its use in the early 1990s [21] , where the measured field-effect hole mobility was 2×10^{-3} cm^2/Vs, with further demonstrations of its deposition by molecular beam [22] (mobility 0.038 cm^2/Vs) or from a solution deposited precursor [23] (mobility: 1×10^{-3} cm^2/Vs on silicon nitride and 9×10^{-3} cm^2/Vs on SiO_2) following in subsequent years. After the early initial developments and advances in reported mobilities

of pentacene TFTs reported enhancements have tended to saturate, with little advance in recent years. The highest reported mobility in pentacene TFTs is 6.3 cm^2/Vs [20].

However, while headline performance figures have not been discussed to the extent that those of a new material will be, there has been a wide ranging field of literature develop which has explored many of the characteristics of pentacene devices when applied to real world use scenarios, such as in RFID tags [24], under continued use [25], with novel gate dielectrics [26] or with surface treatments [27]. Furthermore, the fact that performance is so well characterised has enabled research to be carried out building understanding on a wide platform, using pentacene as a representative material for the class of small molecule organic semiconductors. As such, pentacene is one of the most widely studied organic semiconducting materials, making it an excellent choice to explore device architecture, dielectric composition and surface treatment variations and combinations.

1.1.2.2 Copper Phthalocyanine

Another widely studied organic semiconductor, copper phthalocyanine, has its origins in the dye industry, where it was discovered in 1928 [28], with a full description published over the subsequent few years by Linstead [29], who also developed a number of other metal phthalocyanine variants. Having been discovered by accident by workers in the dye industry, it was soon put to good use as a highly stable blue pigment, exploiting the significant optical absorption in the low energy part of the visible spectrum (red).

CuPc was first considered as a semiconductor in 1948 [30], and has received significant attention for applications in catalysis [31], gas sensing [32, 33], optoelectronics [34, 35, 36, 37] (largely thanks to its high absorption in the visible range), in field effect transistors [38, 39], and more recently in spintronics [40].

While a majority of the semiconducting uses of CuPc have tended to be in the optoelectronic area, commonly as electron acceptors in hetero-junction photovoltaic devices, of particular interest to us are the reports of use in field effect transistors, where mobilities as high as 0.1 cm^2/Vs have been reported [41], with

values more commonly around 10^{-2} cm^2/Vs [38]. Some more recent work has also shown CuPc to display significant photoconductivity [42].

A further aspect of recent interest is that of the formation of novel CuPc nanowires [6], with similar wires also being considered for use in transistors [43] and as photoswitches [44].

1.2 Further Opportunities for Novel Applications

1.2.1 One-dimensional materials

As mentioned above, the application of organic semiconducting materials is threatening to extend beyond the traditional applications of TFTs, such as in displays, where there is significant disruptive potential, and into areas of technology previously dominated by more exotic inorganic materials. It is perhaps the ability of organic materials to self-assemble over large length scales [6], that can be of most use here. While traditional photolithography and fabrication techniques are becoming stretched to their limits (and beyond) to enable nanostructured devices to be fabricated in conventional inorganic materials [45], careful selection of growth conditions can yield organic nanowires which would take months of dedicated electron-beam lithography (EBL) to produce in a silicon sample in a number of hours. Furthermore, these organic nanowires can be free from substrates, and possess incredible mechanical strength.

While carbon nanotubes (CNTs) have led the way in the field of organic nanostructures for many years [46, 47] with large scale device integration being demonstrated recently [48, 49], it is perhaps coming to the point where other one-dimensional materials can take on some of what has been learnt in dealing with CNTs, and continue on to more significant achievements with new approaches and applications emerging[50, 51].

CuPc is one such material which is emerging as useful in a one-dimensional form [43, 44], with early reports of electronic transport measurements suggesting significant enhancement in the performance of devices over their equivalent thin

film alternatives. This is one aspect which will be studied in this thesis.

1.2.2 Spintronics

A further field in which organic materials have begun to make an impression is that of spintronics [52]. Materials that exhibit both suitable semiconducting and magnetic properties for spintronic applications have been long sought [53]. By switching from a paradigm of charge-based electronic devices, to spin-based control, it could be possible to increase data processing speed, reduce power consumption and improve integration density over conventional electronic devices. However, materials which allow efficient spin injection and detection, as well as transport, control and manipulation have only begun to be identified and understood in recent years.

Coherent spin has been transported along CNTs [54], while the demonstration of giant magnetoresistance in thin film organic spin-valves [55] has served to prove the potential for organic materials, with many further efforts with organic materials also reported [56].

Of particular interest in this study is CuPc, whose molecules form chain-like stacks enabling efficient spin-entanglement [40]. The molecular arrangement, of a pseudo-one-dimensional chain, can be further enhanced by modifications to the material's structure with even closer molecular stacking observed in the formation of centimetres long nanowires [6], suggesting a route to enhanced spin-entanglement. It is with these magnetic properties in mind that field effect transistors are fabricated with these CuPc nanowires, with a view to providing a platform from which a gate-controlled magnetic device can be fabricated.

1.3 Integration Challenges

While a number of materials and devices have been discussed above, they are all linked by the need for effective integration if they are to succeed in either large area, high volume applications, or as high performance and high value devices. Material properties and processing technologies have advanced at great pace in recent years, but for any such application efficient charge injection is required, as

is a stable substrate onto which a device can be fabricated, or at least mounted, and one which is compatible with the application in mind. Particular challenges are faced with organic devices, not least as possibly the most critical interface, that between an active semiconductor and dielectric, is necessarily exposed to hostile conditions between processing steps, and even where this is avoided to the extent that is possible, an epitaxial interface is not possible, nor is the high quality interface prepared as Si is oxidised to form SiO_2.

1.4 Research Objectives

As organic materials and processing techniques now provide us with a number of novel materials properties the challenge remains to integrate these devices into useful circuits and systems. This work aims to develop an OTFT platform from which novel device applications and architectures can be explored. Use will be made of existing technology and techniques where possible, with adaptations made to accommodate the specific requirements for organic materials. While some advantages can be found by adopting new techniques and materials existing techniques will be examined for their suitability in some cases. Amongst other things this research seeks to:

- Develop OTFT fabrication strategies to provide a universal backplane, allowing simple integration of any organic semiconductor.
- Investigate and optimize PECVD gate dielectrics for use with organic semiconductors.
- Apply the techniques developed to a number of organic materials demonstrating device integration, and the applicability of this modular approach to system design.
- Consider the importance of organic-inorganic interface preparation to organic device performance.
- Explore the transition from thin-film based OFET devices to nanowire devices.

- Examine the performance of nanowire based field effect transistors to establish an understanding of device behaviour.

1.5 Thesis Outline

This thesis is structured as follows: Chapter 2 introduces the operation and fabrication of organic thin film transistors, explaining how key parameters are derived and which characteristics are sought after. Some essential measurement and deposition techniques are also discussed. Chapter 3 focuses on the development of a high quality gate dielectric suitable for OTFT integration while maintaining compatibility with existing technologies. In chapter 4 the fabrication of high performance pentacene OTFTs is described, validating the use of an inorganic dielectric, and allowing the performance of subsequent developments to be compared to the most widely used organic semiconductor. Performance enhancements brought about by surface modification treatments are also discussed. The fabrication and performance of CuPc TFTs are briefly discussed in chapter 5, which then goes on to explore at length the applicability of a TFT approach to the fabrication of CuPc NW FETs, while also developing a number of novel device analysis techniques. Finally, chapter 6 examines the achievements to date, and describes some avenues of further research which this research suggests should yield exciting results.

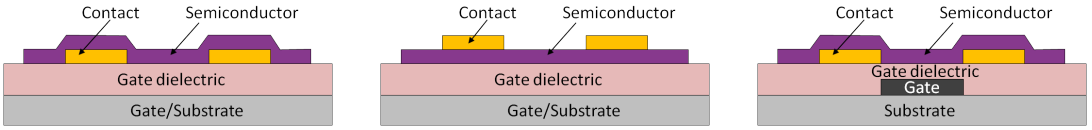
Chapter 2

Organic Thin Film Transistor Overview

OTFTs, or more generally TFTs, vary significantly from conventional metal-oxide-semiconductor field-effect-transistors (MOSFETs) fabricated from crystalline silicon and typically employed for most integrated circuit applications. While MOSFETs typically operate in under inversion, a TFT generally operates in accumulation. However, this is brought about in a similar fashion in both classes of device, by the application of an electric field across a gate dielectric. While a MOSFET's channel will initially become entirely depleted of majority carriers, before entering inversion, a TFT will simply accumulate charge close to the semiconductor-dielectric interface, the polarity of which is defined by the applied gate voltage. As such, it is possible for either n-type or p-type TFTs to operate with identical structures, unlike MOSFETs.

2.1 OTFT Device Architecture

Several architectures exist for OTFTs, and can be used depending on processing limitations. While in some instances it may be beneficial to use a bottom contact arrangement (2.1a) this requires the semiconducting layer to be deposited after the contacts. However, if top-contact is chosen, the semiconducting layer may be exposed to harsh process conditions required for the deposition or patterning of



(a) Bottom contact bottom gate OTFT

(b) Top contact bottom gate OTFT

(c) Bottom contact bottom gate OTFT with discrete gate

Figure 2.1: Common OTFT architectures

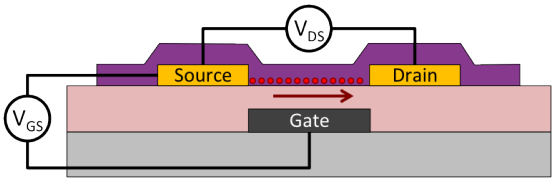


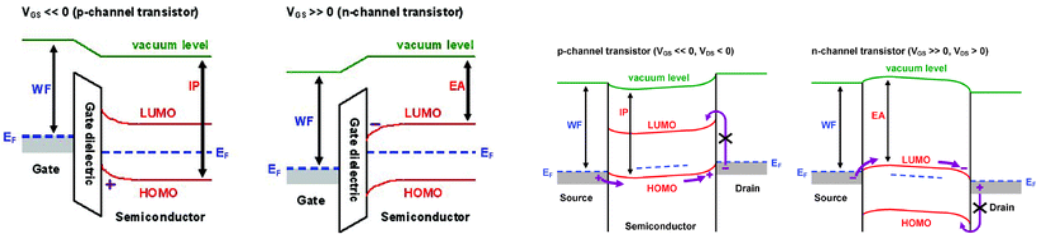
Figure 2.2: Schematic OTFT under applied gate and drain bias showing charge accumulation and transport. For n-type device $V_{GS} > 0V$, $V_{DS} > 0V$. For p-type $V_{GS} < 0V$, $V_{DS} < 0V$.

the contacts. For device integration it is necessary to consider all future processing requirements, ensuring that any damage to device performance is avoided. In this work we focus on the use of bottom-contact bottom-gate (BCBG) OTFTs, to preserve the semiconducting layer once deposited.

Both bottom- and top-contact transistors as described above can be investigated on a small scale using a common gate, provided by the substrate material. However, device integration is impossible without individually addressable TFTs, meaning that a discrete gate is necessary for every device. By using an insulating substrate and defining a gate metal layer before dielectric deposition this can be achieved, allowing either bottom-gate or top-gate architectures to be used, with a bottom-contact discrete bottom-gate device shown in figure 2.1c.

2.2 OTFT Operation

A thin film transistor operates by coupling an applied gate-source voltage across a dielectric layer, accumulating charge in a semiconducting later as shown in figure 2.2. This sheet of induced charge carriers is mobile, and can be caused to flow through the semiconducting layer by the application of a second voltage



(a) Interface band bending **(b)** Channel band alignment

Figure 2.3: Energy-level diagrams illustrating the operation of p- and n-type OTFTs [2].

bias, now between the drain and source. The density of charge carriers induced is heavily dependent on the gate-source voltage, and consequently the drain-source conductivity can be modulated by a change in gate-source voltage.

Figure 2.3a shows energy-level diagrams at the crucial semiconductor/dielectric interface. For a p-channel (n-channel) device it can be seen that as a negative (positive) gate voltage is applied, the HOMO (LUMO) level is bent in close proximity to the dielectric interface such that it approaches the fermi-level of the material, inducing charge in a sheet at the interface.

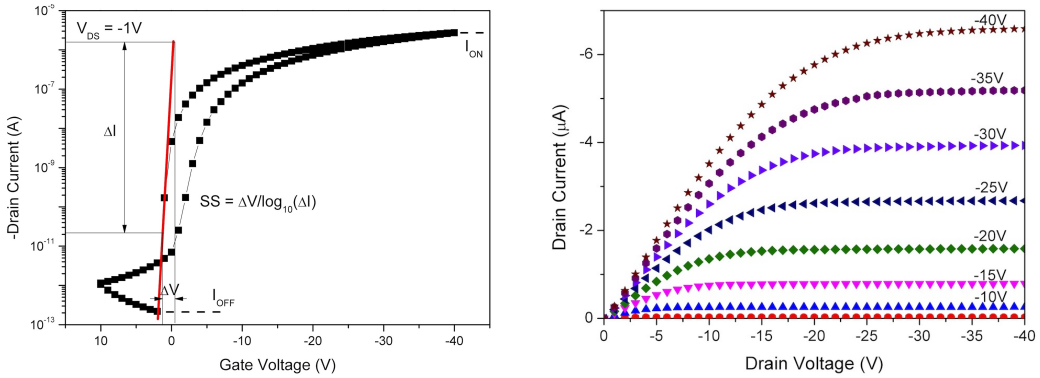
Figure 2.3b shows further energy-level diagrams, but now along the length of a channel, showing the potential seen by a charge-carrier as it traverses the channel region from source to drain. It can be see that the large band offset for one polarity of carrier in each device ensures that each device is only either p- or n-type, and that ambipolar operation is hard to achieve.

2.3 OTFT Characteristics

For low drain-source voltages (V_{DS}), the current flowing through the channel of a TFT, between drain and source, should be linear with V_{DS}, and is given by:

$$I_{DS,lin} = \mu_{FE} C_i \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \tag{2.1}$$

Where I_{DS} is the drain-source current, V_{GS} is the gate-source voltage, V_T is the threshold voltage, μ_{FE} is the field-effect mobility, C_i the capacitance per unit area of the gate dielectric and W and L the channel width and length respectively.



(a) Transfer ($I_D - V_{GS}$) Curve **(b)** Output ($I_D - V_{DS}$) Curve

Figure 2.4: Typical electrical characteristics of a p-type OTFT

For larger V_{DS} the device enters the saturation regime and I_{DS} becomes independent of V_{DS}, with I_{DS} now approximated by:

$$I_{DS,sat} = \frac{1}{2}\mu_{FE}C_i\frac{W}{L}\left(V_{GS} - V_T\right)^2 \tag{2.2}$$

The transition from linear to saturation behaviour is visible in the output characteristics of Figure 2.4b.

All TFTs are characterised using two simple measurements. The first, the transfer ($I_D - V_{GS}$) characteristic, is performed by sweeping the transistor's gate voltage while measuring the current flowing through the channel for a fixed V_{DS}. The second, the output ($I_D - V_{DS}$) characteristic, requires V_{DS} to be swept for a series of gate voltages, and I_D to be measured. Examples of both are shown in figure 2.4.

The two equations above generally describe the behaviour of TFTs, with the efficiency of charge-transport (μ_{FE}) taken as a figure of merit describing the transport in the channel of the device. A second significant consideration is the charge injection efficiency, characterised by contact resistance (R_C).

2.3.1 Parameter Extraction

Equations 2.1 and 2.2 are used to approximate OTFT characteristics, allowing comparisons to be made between different devices. While these equations do

make several assumptions the are consistently applied to all devices considered.

2.3.1.1 Threshold Voltage

The threshold voltage can simply be extracted by plotting $I_{DS,lin}$ and fitting a straight line to the linear portion of the curve, with the intercept being the threshold voltage.

2.3.1.2 Field Effect Mobility

Field effect mobility is extracted from transconductance ($g_{m,lin}$), which is derived from equation 2.1 as follows:

$$g_{m,lin} = \frac{\partial I_{D,lin}}{\partial V_{GS}} = \mu_{FE,lin} C_i \frac{W}{L} V_{DS} \tag{2.3}$$

It follows that the mobility in the linear regime can be extracted from $g_{m,lin}$ as follows:

$$\mu_{FE,lin} = \frac{g_{m,lin}}{C_i V_{DS}} \frac{L}{W} \tag{2.4}$$

And similarly in the saturation regime, transconductance can be defined as follows:

$$g_{m,sat} = \frac{\partial I_{D,sat}}{\partial V_{GS}} = \mu_{FE,sat} C_i \frac{W}{L} (V_{GS} - V_T) \tag{2.5}$$

By rearranging equation 2.2 it is possible to derive an expression for field-effect mobility in the saturation regime, which can be particularly useful where contact problems result in poor device characteristics in the linear regime:

$$\mu_{FE,sat} = \frac{2L}{C_i W} \left(\frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2 \tag{2.6}$$

2.3.1.3 Sub-threshold Slope

The inverse sub-threshold slope (SS) and I_{on}/I_{off} can be extracted from the I_D-V_{GS} curve, as illustrated in figure 2.4a. The SS provides a measure of how well the device turns on and off, and can be closely related to the density of states

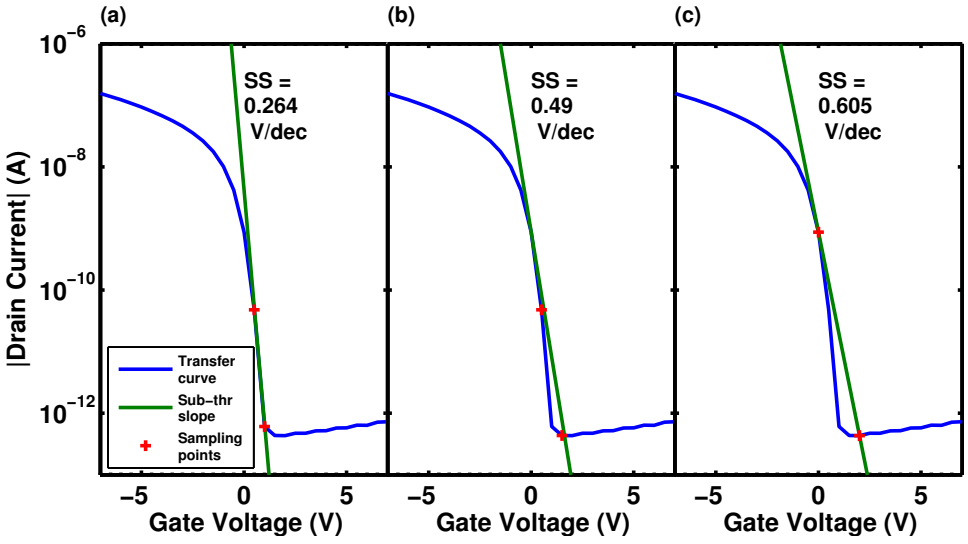


Figure 2.5: Sub-threshold slope extraction and errors.

at the dielectric-semiconductor interface in thin film transistors. While a large slope (small SS value) is a desirable characteristic, extraction of this parameter can be subject to significant estimation errors. Due to the fact that any transfer curve measurement will be taken as a series of discrete steps, the step size can have a significant effect on the measured SS, especially when it is considered that the maximum slope may occur over a very small voltage range.

A simple visualisation of this sampling error is presented in figure 2.5, where the same characteristic is shown to have a SS ranging from 0.26 V/decade (figure 2.5 (a)) to 0.61 V/decade (figure 2.5 (c)) depending on the sampling resolution chosen. While a smaller step size is beneficial in this regard, it will also lead to a slower measurement, and possible charge trapping from distorting device behaviour in other ways, which would not lead to a true representation of device performance. For this reason, a compromise must be found between accuracy of measurement and speed of data collection.

2.3.1.4 Contact Resistance

Contact resistance (R_C) provides a simple means to describe the efficiency of carrier injection at the metal-semiconductor interfaces. A transmission line method is used to separate channel and contact resistances as follows, using techniques

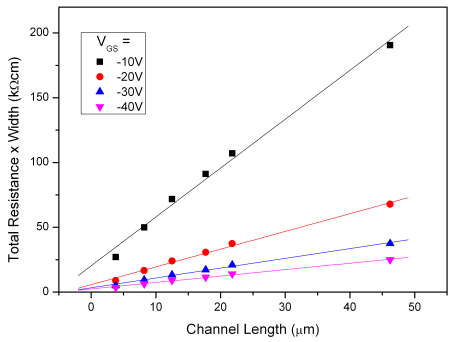


Figure 2.6: Contact resistance extraction for pentacene OTFT

developed in the study of amorphous silicon TFTs [57] but also widely adapted for use with organic materials [58]:

$$R_{TOT} \cdot W = R_C \cdot W + \frac{L}{\mu_{FE} C_i \left(V_{GS} - V_T\right)} \tag{2.7}$$

Where R_{TOT} is the total, or terminal resistance and R_C is the extracted total contact resistance $(R_S + R_D)$. An example plot of R_{TOT} versus channel length is shown in figure 2.6.

The total contact resistance extracted can further be observed to reduce with increasing gate voltage. As such, it can be understood to be a made up of a gate voltage independent effective contact resistance $(R_C W)_0$ in series combination with a gate voltage dependent term, as derived by Luan and Neudeck in their work with amorphous silicon TFTs:

$$R_C \cdot W = \frac{L_0}{\mu_{FE} C_i \left(V_{GS} - V_{T,c}\right)} + (R_C \cdot W)_0 \tag{2.8}$$

When using this model, $(R_C W)_0$ is associated with a hole injection barrier, while the variable term is modelled as an accumulation channel resistance of length L_0. In extracting these values, L_0 is in fact the negative length at which the regression line of total resistance with channel length intercepts the zero-resistance axis. This portion of contact resistance can be seen to be related to inhibited transport of charges from the electrodes to the accumulation region [59], and will strongly depend on the local morphology of the semiconductor, which

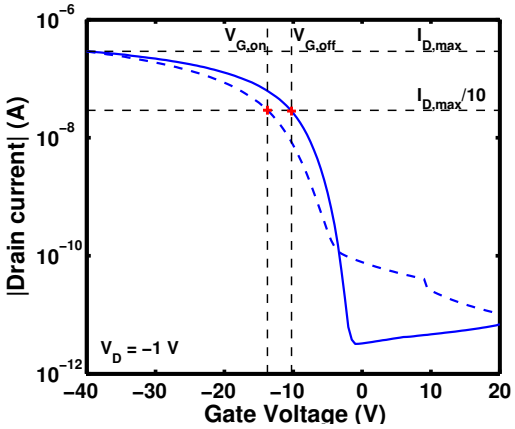


Figure 2.7: Hysteresis extraction for pentacene OTFT

in the case of bottom contact OTFTs can itself strongly depend on the precise device geometry.

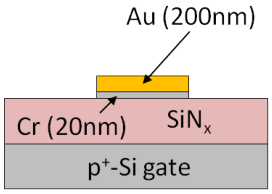
2.3.1.5 Hysteresis

A further parameter which can be usefully extracted from TFT characteristics is hysteresis. While this is difficult to use as an absolute measure of device performance, due to its transient nature, it can provide a useful comparative tool between otherwise similar devices. Also, while a number of possible definitions exist, one has been selected to enable a systematic comparison to be made between a large number of devices. This method is illustrated as applied to a pentacene TFT in figure 2.7, where the difference on turn-on voltage and turn-off voltage is extracted when the devices drain current passes through 10 % of the maximum on-current.

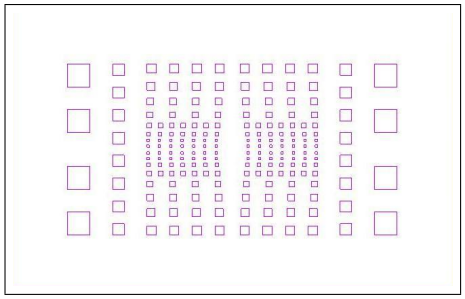
2.4 OTFT Fabrication Techniques

2.4.1 Mask Design

To enable material and device characterisation various masks for OTFT and test structure fabrication were designed. A simple shadow mask is used for large features (minimum feature 200 μm) while a chrome coated glass mask is used for



(a) Schematic cross section of electrical test structure



(b) Electrical test structure mask layout

Figure 2.8: Electrical test structures

features as small as 5μm.

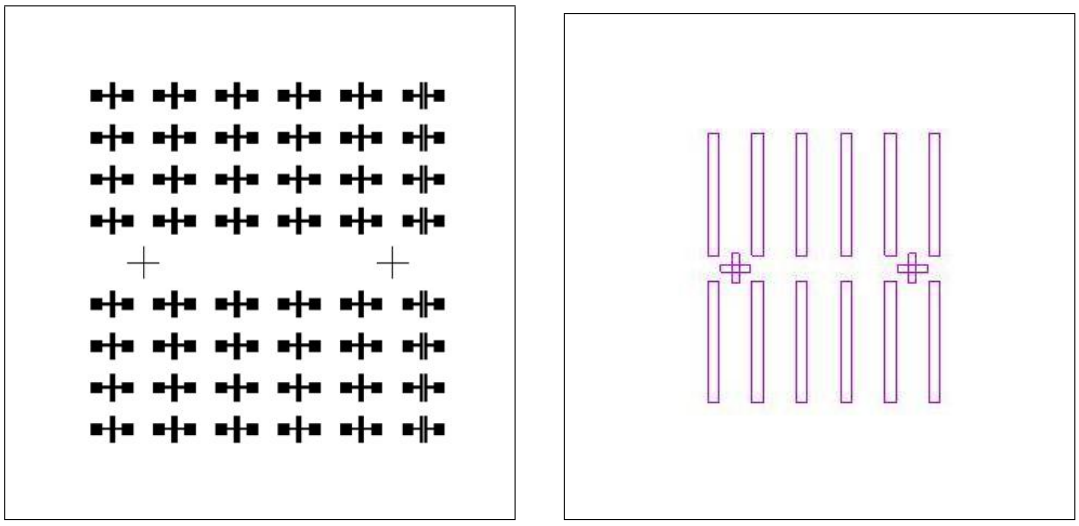
2.4.1.1 Two Terminal Current-Voltage

Test structures for electrical measurements were fabricated using a highly conductive silicon substrate as one electrode, with a second electrode formed on top of the film by the evaporation of a chromium/gold bi-layer through a shadow mask. Chromium provides a good electrical contact, without suffering from the diffusion that metals such as aluminium may exhibit. Gold is used as a second layer to provide a thick contact onto which probes can be lowered, without risking scratching the surface. The structure of these devices is shown schematically in figure 2.8a.

The shadow mask used was designed for this purpose, and contains several square openings of sizes ranging from approximately 2mm to a smallest feature of 200μm, as limited by the mask fabrication process. Figure 2.8b shows the design layout.

2.4.1.2 Thin Film Transistor Contact Definition

A simple single layer optical lithography mask for BGBC OTFTs was designed to allow several pairs of transistor contacts to be fabricated in parallel. The mask is shown in figure 2.9a, with 8 rows of 6 different transistor geometries patterned



(a) Source and drain contact definition by optical lithography mask

(b) Organic film definition by shadow mask

Figure 2.9: OTFT contact definition masks

on each 10 mm square chip. The 6 devices all use the same channel width of 500 μm, but have channel lengths of approximately 5, 10, 15, 20, 25 and 50 μm. This allows contact resistance to be simply extracted by the method described above (2.3.1.4).

This mask is used in conjunction with a simple shadow mask (figure 2.9b), to enable organic layers to be patterned, reducing the possibility for leakage currents to exist between devices.

2.4.2 OTFT Integration

A further set of masks were designed containing a large number of test structures, thin film transistors and simple integrated circuits. These will be used, in conjunction with a custom shadow mask to isolate islands of organic material, to fabricate devices as shown in figure 2.1c once all materials and processes have a been fully developed.

Chapter 3

Plasma Enhanced Chemical Vapour Deposited Silicon Nitride Gate Dielectric Optimization

Integral to any form of field effect transistor is a gate dielectric, across which a field is applied, allowing charge accumulation, or depletion, to occur at the dielectric semiconductor interface. As such, the performance of this material is crucial to the operation of the device, and it must not be neglected in the consideration of new device structures and semiconducting material choices. While silicon based complimentary metal oxide semiconductor (CMOS) processes regularly use thermally grown SiO_2, or more recently ultra-thin high-k dielectrics, to form a high quality gate dielectric, these choices are unavailable to thin film transistor designers due to the requirement of crystalline silicon as a growth substrate.

A thin film transistor's gate dielectric must provide a high resistivity barrier between gate and channel, while also possessing a high dielectric strength, to enable significant charge accumulation to occur. Furthermore, it must present an interface compatible with both previous and subsequent processing steps, to enable successful device integration. Finally, its processing must satisfy the requirements of the specific application of the circuit being fabricated, be that thermal budget, large area uniformity or some other constraint, such as mechanical flexibility.

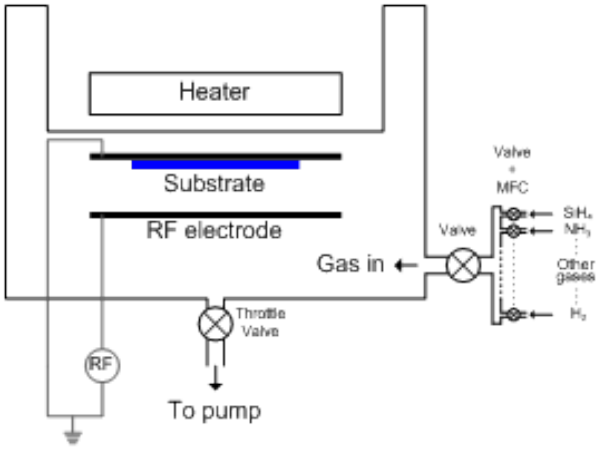


Figure 3.1: Schematic illustration of a PECVD deposition chamber.

Active matrix TFT displays and imagers are commonly based on amorphous silicon and routinely utilize a silicon nitride (SiN_x) dielectric deposited by plasma enhanced chemical vapour deposition (PECVD) [60, 61, 62], chosen for its low leakage characteristics and high dielectric constant, and potential for low temperature, large area and high throughput deposition. However, as more attention has been focused on organic active materials in recent years, the platform so successful for use in amorphous and nc-Si devices has failed to be widely adopted. This work explores the application of SiN_x to OTFTs.

3.1 Experimental Details

PECVD is a chemical vapour deposition technique in which ionic species chemically react at the surface of a deposition substrate, resulting in a film being deposited. Precursor gases are introduced into a reaction chamber, typically under moderate vacuum, after which a plasma is generated by the decomposition of the gases under the influence of a radio frequency power source. A typical chamber is shown schematically in figure 3.1.

All SiN_x films investigated in this work were deposited by PECVD, using a multi-chamber parallel plate system from M V Systems, with a 13.56 MHz radio frequency source. A resistive heater arranged above and outside the chamber enables an elevated temperature to be maintained inside the chamber, although

the indirect coupling necessitates a pre-heat duration before a substrate will reach the desired temperature. For this work, a pre-heat period of 30 minutes was used before every deposition.

Films were deposited on a number of substrates to enable various characterisation methods:

- Highly doped (low resistivity) crystalline silicon for thickness and electrical measurements,
- Chromium coated glass for pinhole density measurements,
- High purity (high resistivity) crystalline silicon for FTIR investigations,
- Quartz for UV-visible absorption.

Prior to deposition substrates were cleaned in a sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) solution (piranha clean)to remove any organic contaminants before being thoroughly rinsed in deionized (DI) water. All silicon substrates were also dipped in buffered hydrofluoric (HF) acid to remove any surface oxide, before being rinsed in DI water and blown dry with dry nitrogen gas.

Initial plasma conditions were based on work carried out on a similar system by Li et al. [63] however as conditions can vary from one system to another it is not possible to transfer a recipe directly. Initially films were deposited at 300 °C, with a variety of film compositions considered for device applications. While film composition was varied by altering the silane (SiH_4) and ammonia (NH_3) gas flow rates all other parameters (such as pressure, substrate temperature and RF power) were kept constant. The process conditions investigated for 300 °C are summarized in table 3.1.

Further to this process conditions were investigated and optimized for SiN_x deposition at 150 °C, a temperature compatible with flexible plastic substrates (e.g. PEN, PET) [60]. While several reports do exist of 150 °C nitrides there are few materials successfully used in organic devices [64]. One previous report of such low temperature material studies the effect of varying material composition on the performance of solution processed organic TFTs [63]. Here we explore

Parameter		Unit	Value	
Substrate temperature		(°C)	300	150
Process pressure		(T)	0.4	1
RF Power		(W)	2	5-40
Gas flow rate	SiH_4	(sccm)	4	2
	NH_3	(sccm)	20-80	10-40
	H_2	(sccm)	0	0-80
	N_2	(sccm)	0	0-80
	He	(sccm)	0	0-80

Table 3.1: Process conditions for silicon nitride at 150 °C and 300 °C

dielectric properties in relation to vacuum deposited (i.e. small molecule) organic semiconductors.

The process conditions considered for 150 °C silicon nitride are summarized in table 3.1, along with those for the higher temperature deposition. The key difference in conditions from the higher temperature deposition was the introduction of dilutant gases, in the form of H_2, N_2 or He.

3.2 Thin Film Characterisation

Silicon nitride films were characterised by a number of methods prior to being integrated into devices. Various techniques were used to examine the deposition of the films and also the structural, surface and electrical properties. The deposition rate was examined and related to deposition conditions. Bulk and structural properties, such as the chemical bonding structure were investigated by use of Fourier-Transfer Infrared spectroscopy (FTIR), while film thickness was measured by ellipsometry. Film density was estimated by monitoring mass change. The film surfaces were characterised by atomic force microscopy (AFM). Electrical properties were characterised by measuring metal-insulator-semiconductor (MIS) structures, with leakage current, breakdown field and dielectric constant of particular interest.

3.2.1 Deposition Conditions

As the deposition conditions are varied for SiN_x growth it is necessary to monitor all aspects of film deposition, as few parameters are truly independent. When varying the gas flow ratios it may also be necessary to adjust RF power to compensate for the energy required to break a larger number of higher energy bonds. Deposition rate is the most easily observed film characteristic, and can be used as a tool to monitor some of the processes involved in material deposition

3.2.1.1 Deposition rate

Initially all SiN_x films were deposited for equal duration (15 minutes), and each film's thickness measured by ellipsometry. Deposition rates were seen to vary as process conditions were varied, as shown in figure 3.2 for a 300 °C deposition temperature.

Far more variation was observed in the development of SiN_x deposition at 150 °C than at 300 °C, with a factor of 3 increase in deposition rate for high NH_3 flow rates over the Si-rich case, whereas for 300 °C films a more modest change in deposition rate suggests a more stable process. Figure 3.3 shows deposition rate as a function of RF power, for several different gas flow ratios for a 150 °C depo-

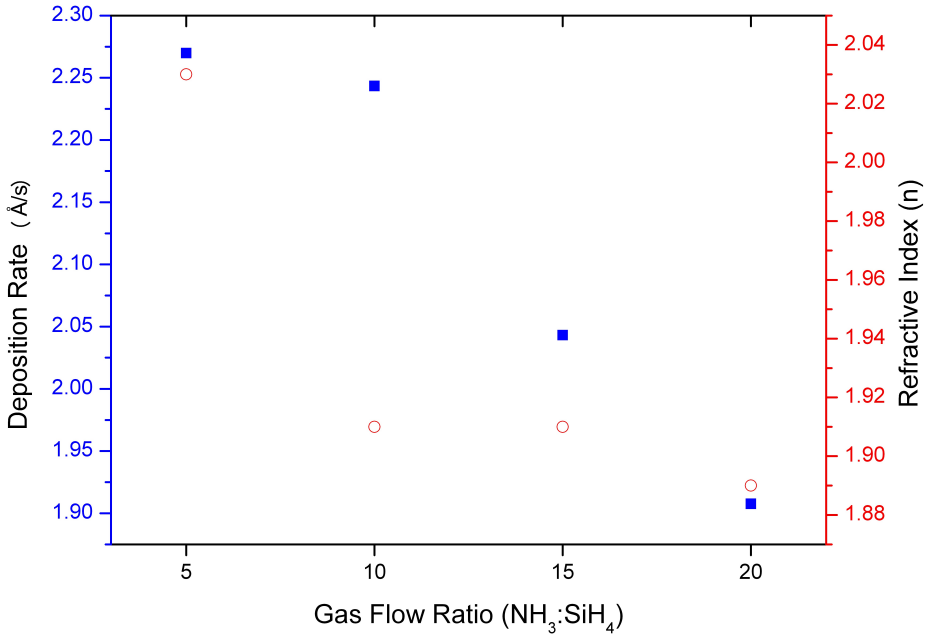


Figure 3.2: Deposition rate and refractive index for SiN_x films deposited at 300 °C

sition temperature. As can be seen for the case of 20:1 NH_3:SiH_4 gas flow there appears to be a peak in deposition rate at 10W of RF power, with rate decreasing both above and below. This trend is not apparent for lower gas flow ratios, where the trend appears to be of increasing deposition rate with power. The concept of a Critical Power (P_C) is introduced by some researchers [65], at which film properties are optimal. Above this power an etching mechanism begins to erode the film as it is deposited, competing with the deposition process, reducing net deposition rate. Considering the need to establish a set of stable deposition conditions for several process conditions, the extremely low deposition rates observed at 10 W for lower gas flow ratios were likely affected by some plasma instability. This instability was observed by variations in plasma bias voltage, and was visible as variations in plasma appearance. As such 10 W plasmas are less likely to exhibit reliably stable and strong materials characteristics.

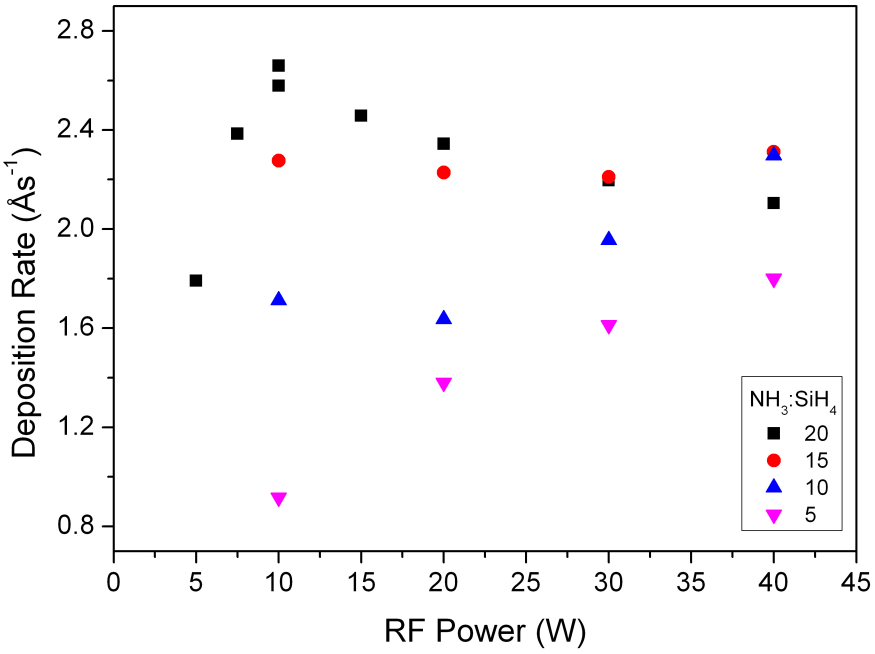


Figure 3.3: Deposition rate for SiN_x films deposited at 150 °C

3.2.2 Structural Characterisation

Silicon nitride in its stoichiometric form is Si_3N_4, however, PECVD SiN_x does not necessarily conform to this requirement, with large numbers of either dangling bond defects, or hydrogen terminated silicon or nitrogen bonds allowing 'x' to vary significantly from below 1.3 (Si-rich) to almost 1.7 (N-rich)[63]. By varying the silicon to nitrogen ratio in the film, it is possible to significantly affect the properties, and as such it is important to understand the relative density of silicon and nitrogen species in each film. One technique allowing such information to be studied is Fourier transform infrared spectroscopy (FTIR), another being observation that a material's refractive index can be correlated to its relative bonding concentration.

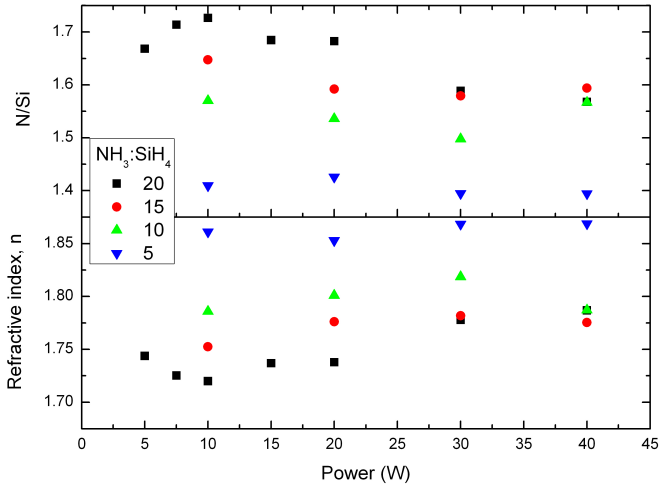


Figure 3.4: Refractive index and [N]/[Si] content as a function of deposition power and gas flow rates

3.2.2.1 Ellipsometry

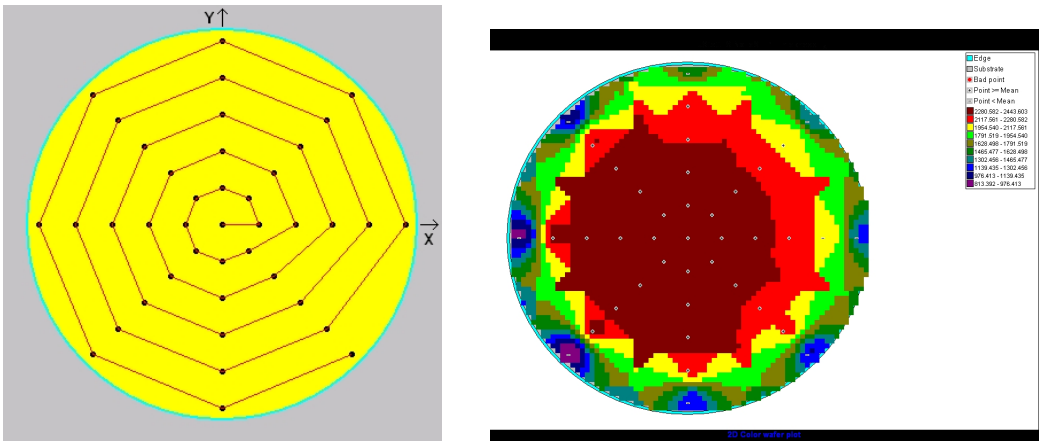
Ellipsometry was used to measure both thickness and refractive index, using Cauchy's empirical equation [66],

$$n = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \tag{3.1}$$

Where A, B and C are constants which are characteristic of any one substance, n is refractive index and λ is the wavelength. This equation was fitted to collected spectroscopic ellipsometry data, with the refractive index for each film to be determined. It has previously been reported that a rise in refractive index can be brought about by increased Si inclusion in SiN_x films [67]. It has also been shown to be possible to estimate the [N]/[Si] ratio for each film from the refractive index (n) using the formula below [68, 69]:

$$\frac{[N]}{[Si]} = \frac{4}{3}\frac{[3.3 - n]}{[n - 0.5]} \tag{3.2}$$

The refractive index, and corresponding [N]/[Si] ratio for each of the 150 °C films is shown in figure 3.4 rising from 1.72 for N-rich films to 1.87 for Si-rich films, with a corresponding decrease in [N]/[Si] from 1.7 to 1.4. The change in [N]/[Si] ratio as the gas composition is changed is clear to see, although it appears



(a) Sample grid **(b)** Contour plot for SiN_x film

Figure 3.5: Thickness mapping by ellipsometry

to be the case that there is little change in composition as a function of deposition power.

While deposition rate was determined by a measurement of the thickness at the centre of each substrate, the variation in thickness across a 3" wafer was measured using a grid of 41 points, arranged in concentric circles of increasing radius, each with 8 points. An example of the grid used is shown in figure 3.5a with an example thickness map also shown in figure 3.5b, mapping the thickness variation of a film deposited at 20W and 150 °C with a NH_3/SiH_4 flow ratio of 20.

Power (W)	NH_3/SiH_4	Average film thickness (%) Radius (mm)					
		0	7	14	21	28	35
10	20	100	99.9	99.5	98.7	96.2	53.9
20	5	100	99.5	98.2	96.0	69.8	25.7
20	10	100	99.4	97.6	95.0	90.8	52.9
20	15	100	99.4	97.4	93.8	88.0	46.3
20	20	100	99.4	98.0	95.5	91.8	47.1

Table 3.2: Average thickness of SiN_x films (percentage of central thickness)

While there is some deterioration in thickness towards the edge of the film, only points on a 35 mm radius circle fall to lower than 90 percent of the cen-

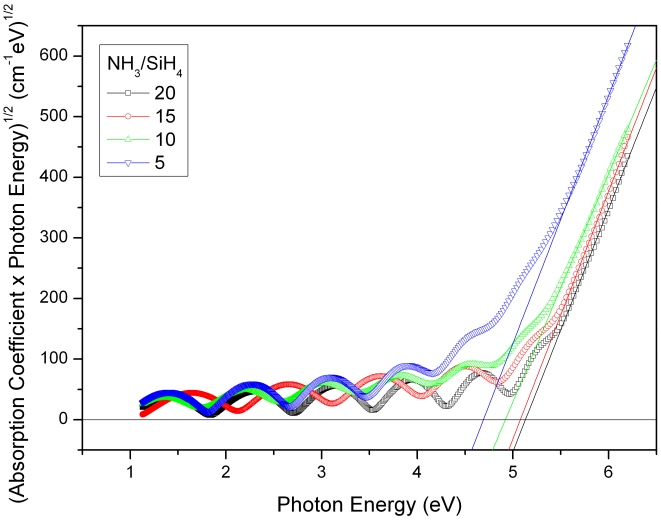


Figure 3.6: Tauc plot for SiN_x films

tre (maximum) thickness for most films deposited on a 3 inch (38mm radius) wafer. Table 3.2 shows a summary of several wafers deposited at difference process conditions, indicating the high uniformity across large areas possible by this deposition technique and with this process. Only the most silicon rich film exhibits significant non-uniformity, with the average thickness falling to 70% at a radius for 28mm from the wafer centre. This can be attributed in part to the same processes which bring about the lower growth rate seen at this process point.

3.2.2.2 UV-visible Absorption

An ultraviolet to visible (UV-vis) absorption spectroscope was used to further characterise the films' properties. By considering the onset of significant optical absorption it is possible to extract the semiconductor bandgap (E_g^{opt}). Clearly for an insulator it is desirable for a large bandgap, preventing the conduction of energetic carriers. A second consideration is that of the band's alignment; if either conduction or valence bands are closely aligned with a semiconductor then some charge transfer and subsequent charge trapping may occur, degrading device performance.

According to the Beer-Lambert law the absorbance in an amorphous material

is given by:

$$A = \alpha d = -\log_{10}\left[\frac{I}{I_o}\right] \tag{3.3}$$

where A is the absorbance, α the absorption coefficient, d the material thickness, I the transmitted light intensity and I_o the incident intensity.

The relationship between absorption coefficient ($\alpha(\omega)$), bandgap (E_g^{opt}) and photon energy ($h\omega$) for amorphous materials is given by [70]:

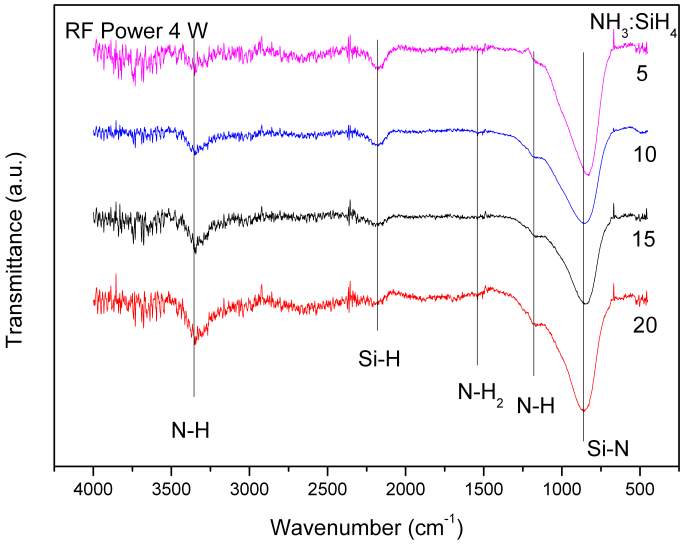
$$\alpha(\omega)\, h\omega = \left((h\omega) - E_g^{opt}\right)^2 \tag{3.4}$$

By plotting $(\alpha(\omega)\, h\omega)^{\frac{1}{2}}$ versus $h\omega$, as in figure 3.6, a Tauc plot, E_g^{opt} can be extracted as the intercept of the linear region with the photon energy. SiN_x films deposited at 20W with various Si:N ratios were examined, with the bandgap showing an increase as the film became more N-rich, with values lowest for the most Si-rich film at 4.7 eV, rising to 5.1 eV for the most N-rich film.

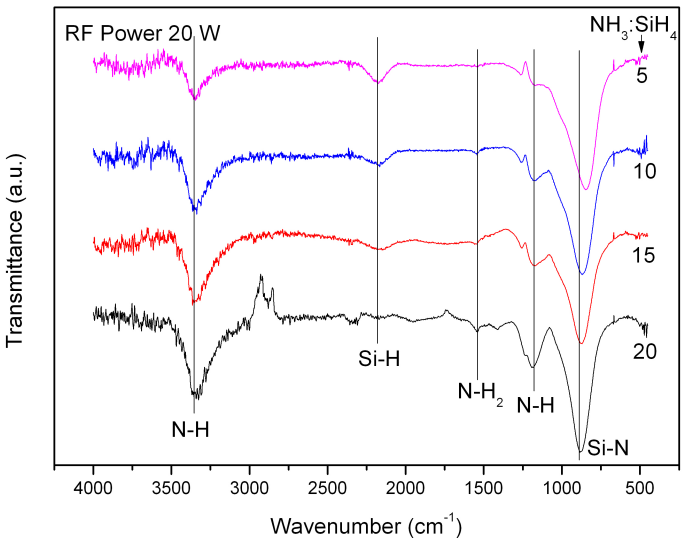
3.2.2.3 Fourier Transfer Infrared Spectroscopy

FTIR spectra were collected using a Perkin Elmer, Spectrum One spectrometer. Films were deposited on piranha cleaned and HF dipped crystalline silicon substrates, with low doping levels (high IR transparency), with a clean substrate used to record a background spectrum before considering SiN_x films. FTIR spectra for 300 °C SiN_x films are shown in Figure 3.7a, with key absorptions corresponding to particular bonding configurations labelled. Figure 3.7b shows the spectra of films deposited at 150 °C, with an RF power of 20 W.

As can be seen in both films, the main absorption peaks are due to S-N bond stretching at around 850 cm^{-1}, N-H bond bending at 1180 cm^{-1} Si-H bond stretching at 2180 cm^{-1} and N-H stretching at 3350 cm^{-1} [71]. From both sets of spectra, it can be seen that as the NH_3/SiH_4 gas flow ratio is increased the N-H stretching and bending modes at 1180 cm^{-1} and 3350 cm^{-1} are both strengthened, while the Si-H bond stretching mode peak at 850 cm is weakened. This gives a clear indication that the film composition is changing, providing qualitative information on bonding composition, to corroborate data extracted from



(a) Films deposited at 300 °C and 4 W RF power



(b) Films deposited at 150 °C and 20 W RF power

Figure 3.7: FTIR spectra of SiN_x films deposited with various NH_3:SiH_4 flow ratios

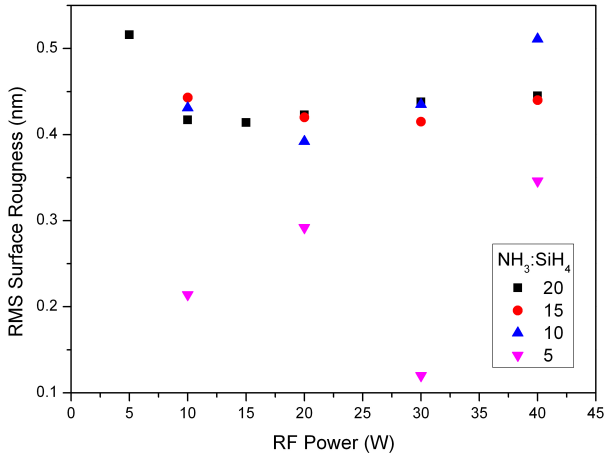


Figure 3.8: RMS roughness of SiN_x films

refractive index measurements. Also worthy of note is the increase in both N-H and Si-H bond strengths for films deposited at 150 °C, showing a higher level of hydrogen inclusion.

3.2.3 Surface Characterisation

3.2.3.1 Atomic Force Microscopy

Atomic Force Microscopy (AFM) allows surface properties to be studied at the atomic level. As deposited SiN_x films were studied by AFM using a Veeco Dimension tool, with MicroMash Ultrasharp 15nm tips.

As can be seen from the AFM images shown in figure 3.9 and summarized in figure 3.8 the surface roughness does not appear to change drastically between films deposited with varying process conditions. Table 3.3 summarizes the roughness of films produced by different deposition conditions. It appears that the deposition power does little to affect the roughness, while the Si:N ratio plays a more significant role, with Si-rich films exhibiting far smoother surface properties than the N-rich alternatives, with the 30 W film having an RMS roughness of just 0.12 nm. However, NH_3/SiH_4 ratios of 10, 15 and 20 all produce films with a similar roughness of approximately 0.42 ± 0.02 nm.

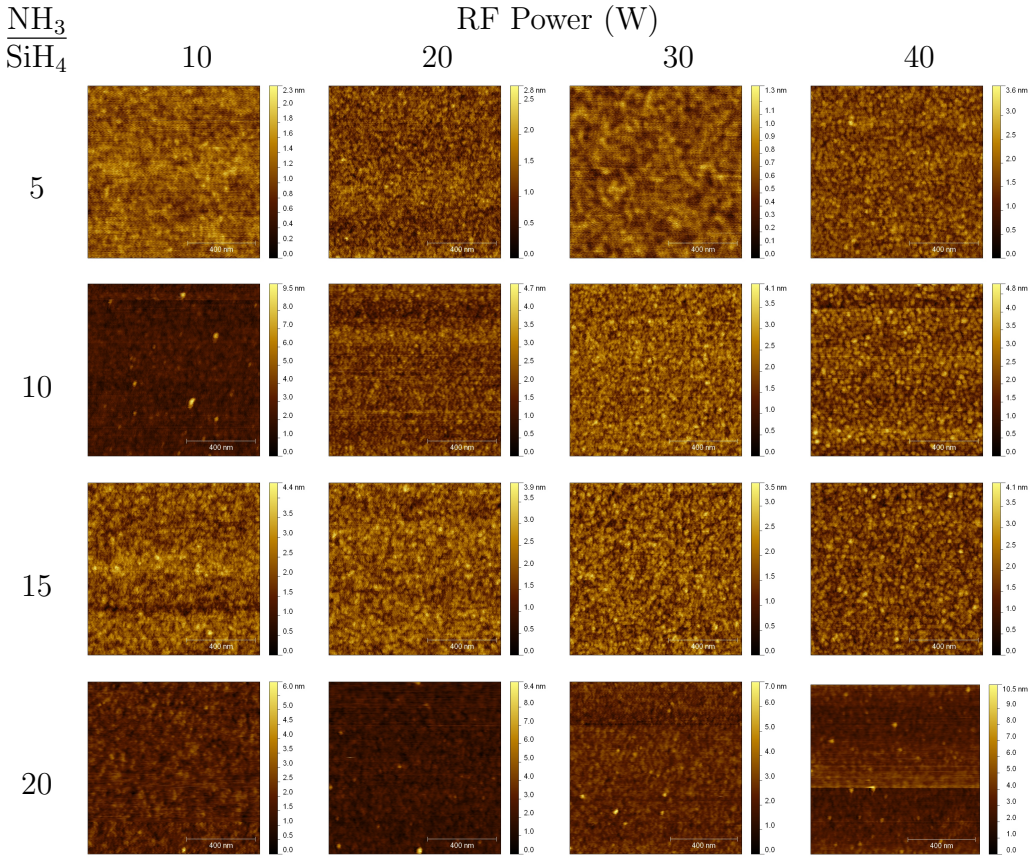


Figure 3.9: AFM images of PECVD SiN_x surfaces with various precursor gas mass flow ratios and RF powers creating varied deposition process conditions. All images show 1 $\mu m \times 1$ μm.

Power	NH_3/SiH_4 flow ratio			
(W)	5	10	15	20
10	0.21	0.43	0.44	0.42
20	0.29	0.39	0.42	0.42
30	0.12	0.44	0.41	0.44
40	0.35	0.51	0.44	0.45

Table 3.3: RMS roughness of SiN_x films

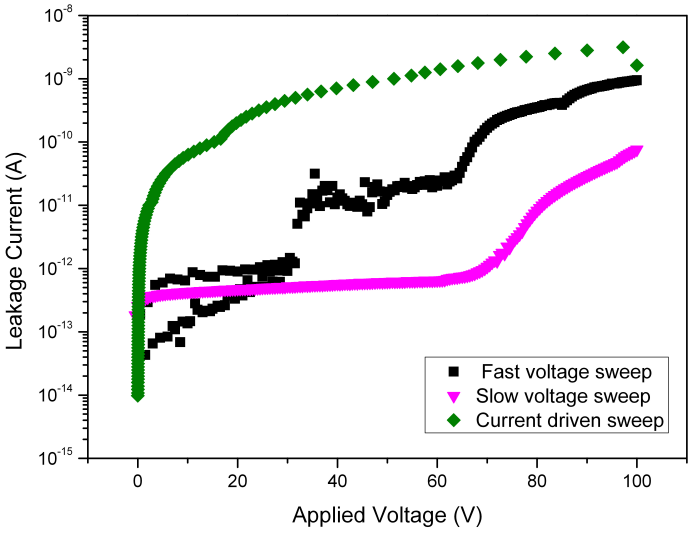


Figure 3.10: Leakage characteristics varying with sweep parameters

3.2.4 Electrical Characterisation

While surface and structural characterisation of SiN_x films are invaluable tools for understanding the underlying structure of films, it is the electrical properties that are a prerequisite for the success of a film as it is these for which the material has been chosen. As such, it is necessary to develop electrical testing protocols to accurately describe the film properties, and to allow some indication of the potential for device performance prior to full device fabrication. As an insulator, it is expected that leakage current through the film will be very small, with a value of 100 pA/cm^2 deemed necessary [72] for device quality material at a typical operating voltage (20V for a-Si:H TFT). Moreover, a gate dielectric material must also enable the accumulation of charge across its thickness, the extent to which this is possible being observed through its dielectric constant.

3.2.4.1 Current-Voltage Measurements

Current-voltage (IV) measurements were carried out using a Keithley 4200 semiconductor characterisation system (SCS) with 4 source-measure units (SMUs), each coupled to a pre-amplifier allowing sub-fA current resolution. This mea-

surement equipment was used in conjunction with a Signatone shielded probe station and triax cabling, allowing excellent noise rejection.

Several testing protocols for measuring leakage current were examined before a routine was established. Each method showed varying results, with a comparison made in figure 3.10. Each sweep was performed on a similar structure, but with either a fast voltage sweep, a slow voltage sweep, or a slow current sweep. It is clear that apparent film properties can vary significantly depending on the measurement protocol followed.

In this instance, it was decided to use a slow voltage sweep, allowing transient properties to settle before the measurement is taken. Any current flow resulting in the charging of low energy traps is hereby ignored, with the current through the film providing the most significant contribution to leakage characteristics.

It was also observed from several repeated measurements that a slow voltage sweep produced the most repeatable characteristics, with breakdown occurring at a similar field for several test structures.

Figure 3.11 shows the leakage current density recorded for an applied electric field of 1 MV/cm on a number of leakage test structures fabricated on films with deposition powers ranging from 5 to 40 W, and with gas flow ratios of NH_3:SiH_4 of 5 to 20, with a significant amount of variation shown between similar films and between devices on one film. What is apparent is that films deposited at 10W, identified as the Critical Power from deposition rate studies, show significant variation in leakage current for most gas flow combinations. For this reason, it was decide to adopt 20 W as the deposition power for further experiments, with the intention that this should provide a stable set of conditions from which to vary other parameters. These initial measurements were performed on film deposited at a single duration, meaning that while they are tested at equivalent electric film strengths, there may be significant variation the film thickness, possibly introducing further variation, as pinhole densities in thinner films may degrade the leakage characteristics. A number of films were subsequently deposited at a uniform thickness of 200nm, allowing a comparison of device quality films to be carried out.

Figure 3.12 shows the leakage characteristics for a number of these 200 nm films deposited at 150 °C and 20 W power. It can be seen there is some con-

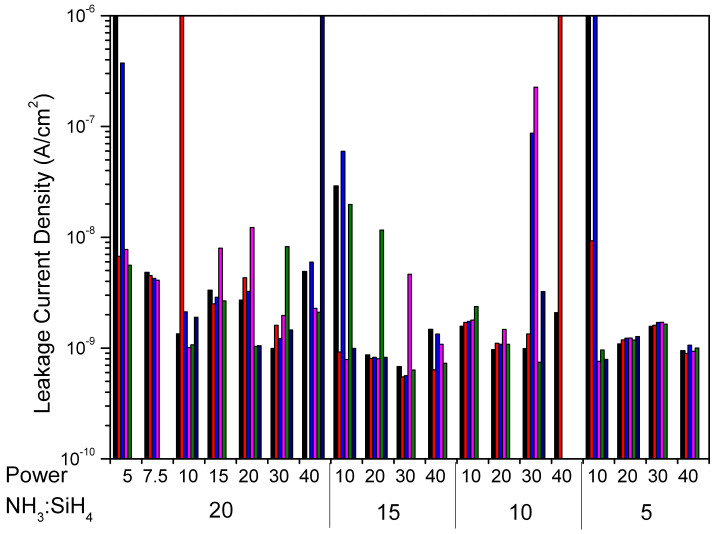


Figure 3.11: Leakage characteristics varying with film properties

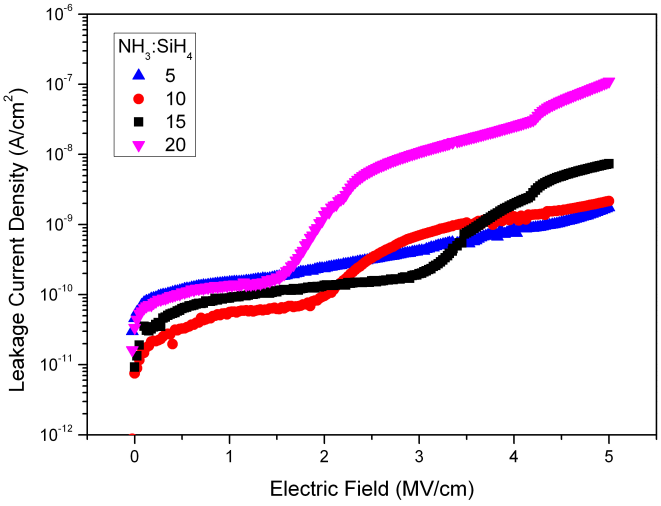


Figure 3.12: Leakage characteristics varying with film properties for films deposited at 20W

siderable variation in the leakage current and also the point at which there is onset of significant leakage. The leakage levels for a large number of SiN_x films are summarised in table 3.4, where the average of several measurements has been taken for each film.

Power (W)	NH_3/SiH_4 flow ratio			
	5	10	15	20
10	1.2×10^{-10}	2.5×10^{-8}	3.7×10^{-7}	3.5×10^{-8}
20	1.5×10^{-10}	5.3×10^{-11}	8.2×10^{-11}	1.9×10^{-10}
30	-	-	6.1×10^{-11}	1.0×10^{-6}

Table 3.4: Leakage current density (A/cm^2) of SiN_x films at 1 MV/cm.

Most 200 nm films deposited at 20 W met the criteria of 100 pA/cm^2, with all showing leakage below 200 pA/cm^2. Significantly higher leakage was seen for 10 W depositions, and more variation for the films at 30 W.

3.3 Conclusions

This work has explored the controlled deposition of silicon nitride films by PECVD, developing reliable process conditions necessary to produce high quality dielectric films for use in organic thin film transistors at a plastic compatible temperature of 150 °C. A study of deposition power on the film deposition rate and film properties yielded a stable power, of 20 W, which was selected for use in all further films. Below this power instabilities were observed in plasma conditions for high silicon content films, while above this power, film variation and leakage properties were seen to increase dramatically. Surface roughness of sub-0.5nm was observed for optimised films, with smoother surfaces being found on Si-rich films. However, the potential gains of a smooth surface, enabling good molecular organisation, and the reduction in surface trap density may well be shown to be negated by the smaller bandgap brought about by the higher Si content, and subsequent lower barrier for carriers becoming trapped within the dielectric itself. This will be investigated by integrating the films into organic thin film transistors.

Chapter 4

Pentacene Thin Film Transistors

Pentacene is possibly the most highly reported organic semiconducting material, due to its relatively high mobility, tendency to form large crystalline grains in thin films and for its relatively high environmental stability when compared to many other organic materials. For this reason, it was chosen as a semiconductor to be used in conjunction with newly developed dielectric materials, as a relatively stable material, with well known and understood characteristics. This choice allows us to investigate surface treatments and compositional changes in dielectric materials, to optimize these steps for use with a variety of materials.

4.1 TFTs with 300 °C SiN_x Gate Dielectric

4.1.1 Device Fabrication

Crystalline silicon wafers coated with either SiO_2 or SiN_x (300 °C deposition temperature, 4 W power, NH_3:SiH_4 20) as gate dielectrics, with lithographically defined Au/Ti contacts as illustrated in figure 2.1a were used as a platform to optimize pentacene device preparation conditions.

4.1.1.1 Surface Treatment

This work is motivated by the intention to transfer some of the techniques commonly employed on SiO_2 dielectric to an integrable platform. Many groups have

demonstrated high performance OTFTs on SiO_2 using a top-contact architecture [73], however it remained unclear whether this strategy could be used on a SiN_x surface. With this in mind devices were prepared to assess the impact of surface treatments, such as exposure to UV-ozone and oxygen plasma, and also to the addition of a self assembled monolayer (SAM).

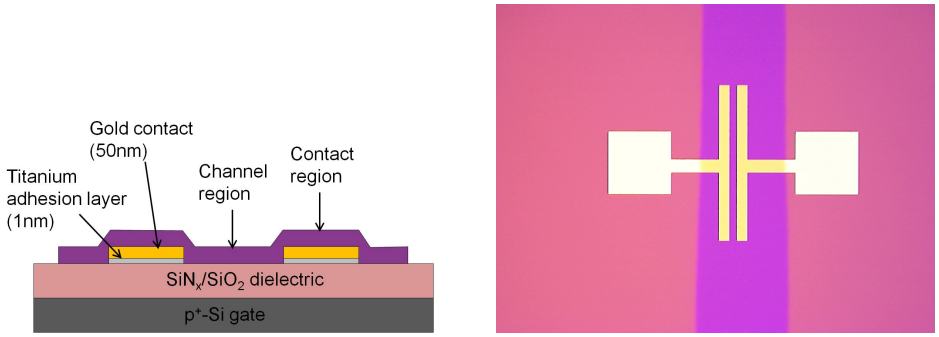
Substrates were initially cleaned with solvents (acetone, isopropyl alcohol) followed by a Piranha clean. This was performed in order to remove any organic material from the surface of both dielectric layer and metal contacts. Once clean the substrates were baked in an oven at 100 °C in order to remove any water molecules adsorbed to the surface during the cleaning process, and then exposed to either an oxygen plasma, or an ozone treatment. A phenyl terminated self-assembled monolayer of β-phenethyltrichlorosilane (PHTS) was formed by the submersion of cleaned substrates in a 10mM solution of PHTS in chloroform in a glove box, with substrates left for a time of 12 hours for the monolayer to fully form, following a process developed by Kumaki et al. for use with SiO_2. [74]. After this substrates were thoroughly cleaned in chloroform, acetone and isopropyl alcohol before being blown dry with nitrogen gas.

4.1.1.2 Pentacene Deposition

All pentacene films were deposited using an ULVAC Evaporator, with a base pressure of $<2\times10^{-4}$ Pa, using a tungsten boat, with twice sublimed pentacene as the source material. Films were deposited at a rate of 0.1 Å/s to a thickness of 40nm. All films were deposited through a shadow mask, allowing patterning of the pentacene layer in accordance with the pre-defined contacts. Figure 4.1b shows an image of one device, with the patterned gold contacts, and stripe of masked pentacene clearly visible.

4.1.2 Device Characterisation and Parameter Extraction

Pentacene devices were characterised in a number of ways, aiming to establish a relationship between the film microstructure and electrical properties of the OTFTs. It was intended to improve the device performance by optimising the organic-inorganic interface, allowing good ordering of pentacene molecules on the



(a) Schematic cross section **(b)** Photograph

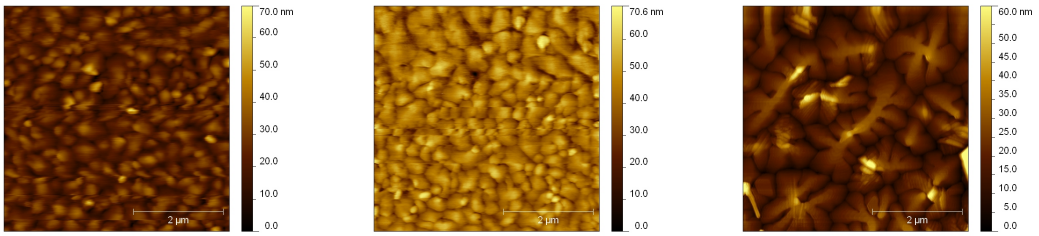
Figure 4.1: A Pentacene Thin Film Transistor.

SiN_x surface.

4.1.2.1 Film Microstructure

Atomic Form Microscopy (AFM) was used to examine in high resolution the pentacene thin film microstructure. A comparison was made between films deposited on SiN_x and SiO_2, and with various surface preparation conditions, such as solvent cleaning, Piranha cleaning, and SAM treatment. Figure 4.3 shows AFM images of pentacene films deposited on SiN_x substrates, in the region labelled as the 'channel region' in figure 4.1a while figure 4.2 shows films deposited on similarly prepared SiO_2 surfaces. A clear trend is visible in both sets of films, with grain sizes increasing as the SAM treatment is applied. Figure 4.5 and table 4.1 summarize the grain size and surface roughness of each set of films, showing the enhancement brought about by the SAM treatment in the film on SiN_x. What is also apparent is the discrepancy between grain sizes on SiO_2 and SiN_x, with grains on SiO_2 being almost twice as large as SiN_x. The largest grains deposited on SiO_2 ($\sim$3 μm) are approaching the minimum channel lengths used for device structures.

A further set of images were gathered for the pentacene film on top of metal contacts, as denoted by the 'contact' region in figure 4.1a. While the transistor channel is formed between the contacts, conduction is often severely affected by the injection barrier from the contact to the film, and as such, the first layers of pentacene on metal must allow for good conduction if efficient carrier injection

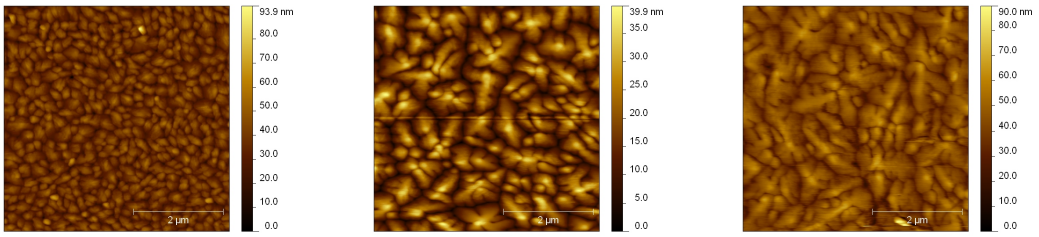


(a) Solvent cleaned substrate

(b) Piranha cleaned substrate

(c) SAM treated substrate

Figure 4.2: AFM images of pentacene on a SiO_2 substrate. Images are 5 $\mu m\times$ 5 μm.

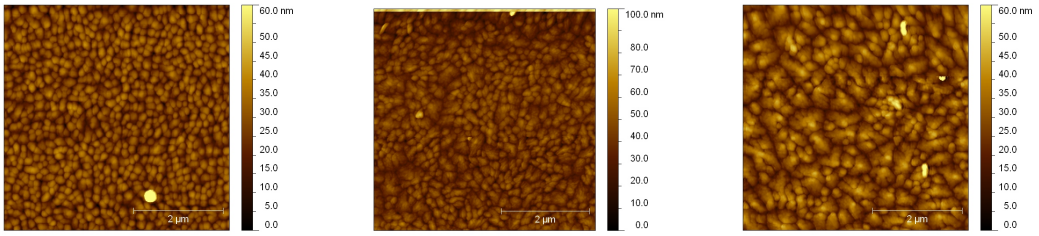


(a) Solvent cleaned substrate

(b) Piranha cleaned substrate

(c) SAM treated substrate

Figure 4.3: AFM images of pentacene on a SiN_x substrate. Images are 5 $\mu m\times$ 5 μm.



(a) Solvent cleaned substrate

(b) Piranha cleaned substrate

(c) SAM treated substrate

Figure 4.4: AFM images of pentacene on Au on a SiN_x substrate. Images are 5 $\mu m\times$ 5 μm.

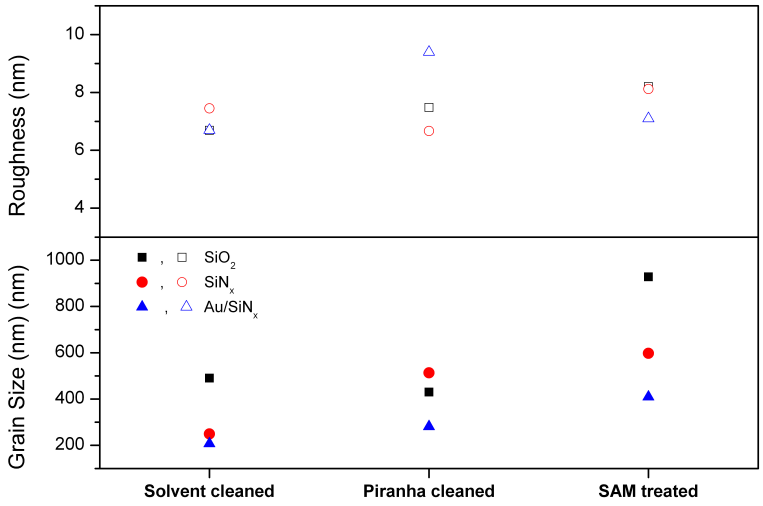


Figure 4.5: Grain size and surface roughness of pentacene films deposited on SiO_2 SiN_x, and Au/SiN_x.

into the channel is to be achieved. Figure 4.4 shows the AFM images of these locations, with significantly smaller grains than equivalent films on dielectric surfaces. Again, film properties are summarised in table 4.1, showing an increase in average grain size from approximately 200 nm on untreated Au contacts to over 400 nm on the SAM treated surface. An unresolved issue remains on the nature of this modification, as the expectation is that the SAM should not effectively adhere to the metal surface, yet an enhancement over the acid treated case is evident.

It is clear that the surface treatments employed play a significant role in allowing a highly ordered film to form on the dielectric surface. However, it remains unclear how this should affect electrical characteristics. It has been disputed whether device mobilities will be enhanced by using larger crystalline grains [75], rather the degree of order at the dielectric-interface appearing to be more responsible for mobility. Moreover, as grain sizes (few μm) approach device channel lengths (5+ μm) it becomes important to monitor uniformity, as the number of grain boundaries impeding transport may be very small, but also may vary significantly along the width of a device, as well as between similar devices.

Substrate	Treatment	Roughness (nm)	Grain size (nm)
SiO_2	Solvent cleaned	6.7	490
	Piranha cleaned	7.5	430
	SAM treated	8.2	928
SiN_x	Solvent cleaned	7.5	249
	Piranha cleaned	6.7	512
	SAM treated	8.1	597
Au/SiN_x	Solvent cleaned	6.7	207
	Piranha cleaned	9.4	281
	SAM treated	7.1	410

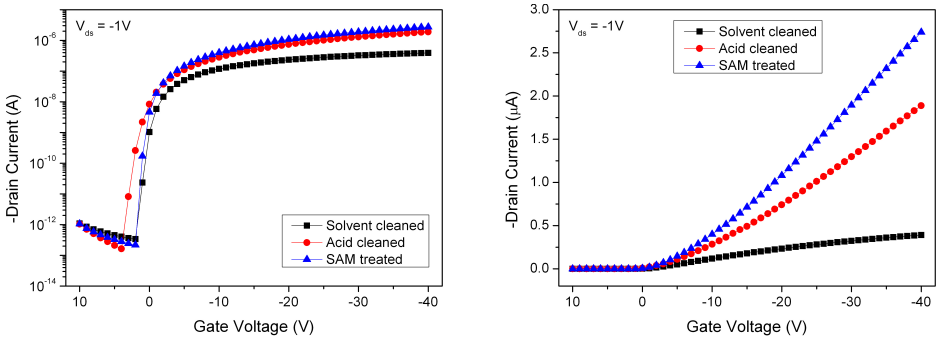
Table 4.1: Film microstructure characteristics of pentacene on various surfaces

4.1.2.2 Electrical Characteristics

Pentacene TFTs were characterised in a vacuum probe station, at a pressure below 1×10^{-5} mbar, using a Keithley 4200-SCS. Transfer and output characteristics were measured for a number of devices prepared in each way. It can be seen from figures 4.6 and 4.7 the effect of cleaning and surface treatment on the operation of the devices on SiN_x and SiO_2. A device on a solvent cleaned substrate is almost an order of magnitude less conductive than a device of the same dimensions where the substrate has been SAM treated. Output curves for the solvent cleaned devices are shown in figure 4.9 with a significant enhancement in the 'on' state visible in the SAM treated alternative devices, with clear saturation behaviour evident for large drain-source voltages.

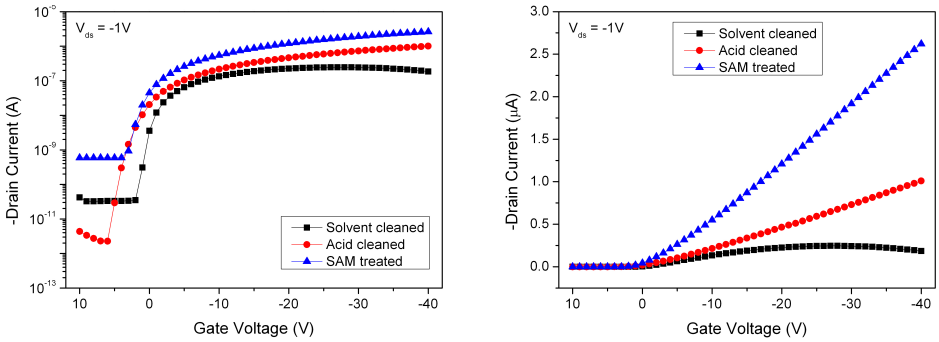
4.1.2.3 Parameter extraction

With transfer and output characteristics available for devices, parameters such as field effect mobility (μ_{FE}), threshold voltage (V_T) and sub-threshold slope (SS) are extracted, and show the significance of the changes brought about by various surface treatments. Table 4.2 summarises these values for devices with matching dimensions. The most significant value here is that of mobility, being increased in the case of the SiN_x device from 0.07 cm^2/Vs to 0.48 cm^2/Vs. However, somewhat surprising is the size of the increase brought about by Piranha cleaning, which brings the value up to almost 0.3 cm^2/Vs. While this is still short of



(a) Logarithmic scale **(b)** Linear scale

Figure 4.6: Transfer characteristics for pentacene TFTs on SiN_x substrates



(a) Logarithmic scale **(b)** Linear scale

Figure 4.7: Transfer characteristics for pentacene TFTs on SiO_2 substrates

the enhancement caused by SAM introduction, it indicates that the process of Piranha cleaning does bring about some surface modification.

One parameter often associated with the dielectric-semiconductor interface is SS [76], which is seen to be reduced (improved) by the surface treatments from 540 mV/decade to 290 mv/decade, while acid treatment appears to cause some degradation to the SS, to 600 mV/decade, although this is subject to some experimental uncertainty, so possibly cannot be deemed to be significant.

Several devices were measured at each process point, allowing contact resistance to be examined using the method described in section 2.3.1.4. Plots of the total resistance for OTFTs on untreated, and SAM treated, SiN_x are shown in figures 4.10a and 4.10b respectively. While the total resistance is greatly reduced

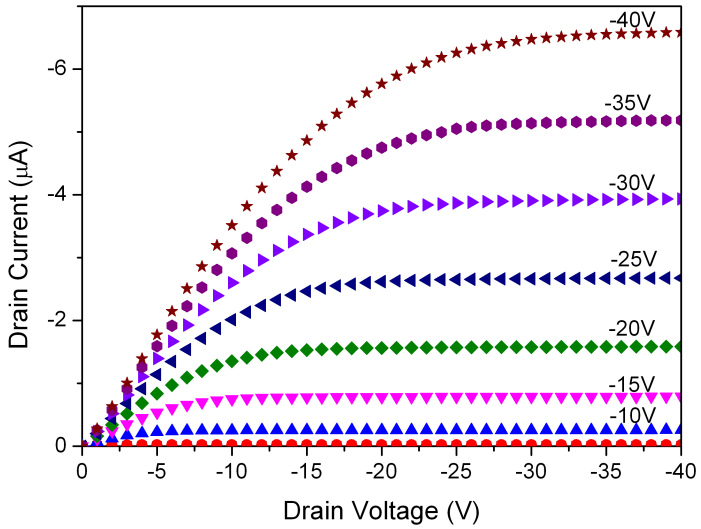


Figure 4.8: Output characteristics of a pentacene TFT on solvent cleaned SiN_x.

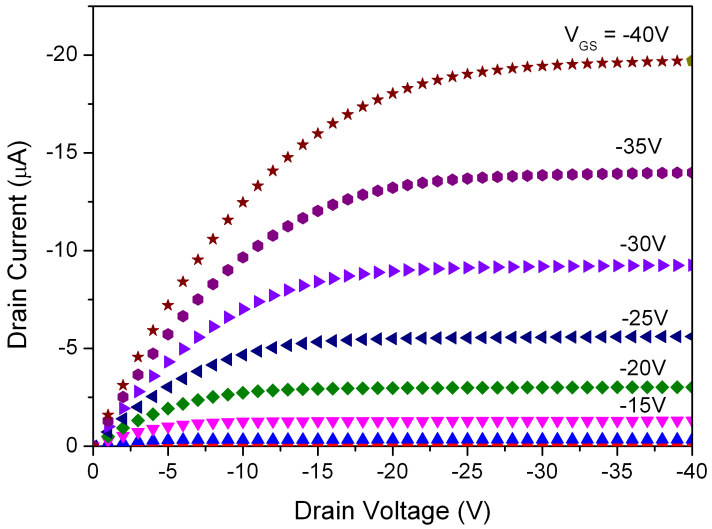
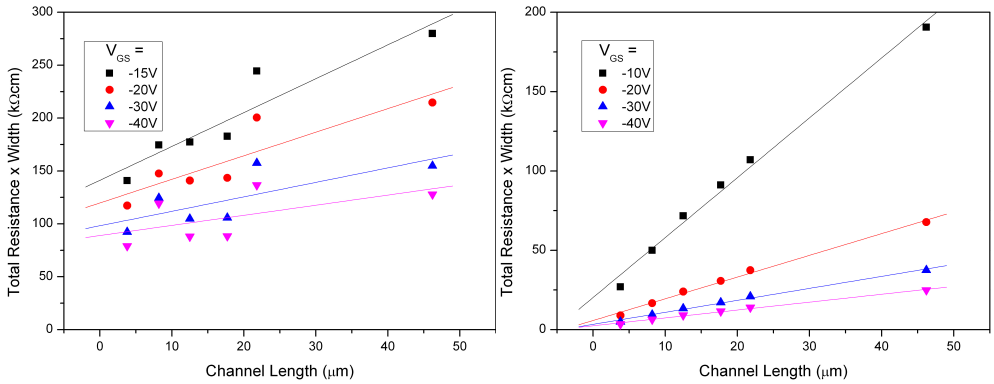


Figure 4.9: Output characteristics of a pentacene TFT on SAM treated SiN_x.

Substrate	Treatment	μ_{FE} (cm^2/Vs)	SS $(mV/decade)$	(I_{on}/I_{off}) -
SiO_2	SAM treated	0.49	480	10^7
SiN_x	Untreated	0.07	540	10^6
	Piranha cleaned	0.29	590	10^7
	SAM treated	0.48	290	10^7

Table 4.2: Pentacene TFT parameter summary. Channel width = 500 μm, length = 46.2 μm.



(a) Untreated substrate **(b)** SAM treated substrate

Figure 4.10: Total resistance for pentacene TFTs on SiN_x substrates at various channel lengths

for each device length in the SAM treated devices the variation is also far less.

From this data it is possible to extract a gate voltage dependent contact resistance, which is plotted for SAM treated SiO_2 devices and several SiN_x devices in figure 4.11. As can be seen, the contact resistance for each set of devices is heavily gate voltage dependent, and is at a minimum for the largest $|V_{GS}|$. The minimum R_C achieved for SiN_x based devices is reduced from over 80 $k\Omega$-cm for untreated surfaces to approximately 2 $k\Omega$-cm for the SAM treated device, with almost identical values seen on SiO_2, and in line with those previously reported for pentacene on SiO_2 [77]. What is perhaps most surprising is the size of the reduction brought about by acid cleaning alone, which reduces the R_C on SiN_x to just 6.5 $k\Omega$-cm, an order of magnitude lower than the untreated case. This indicates that some contact surface modification is likely to have been brought about by the oxidative acid treatment (piranha cleaning). It has previously been

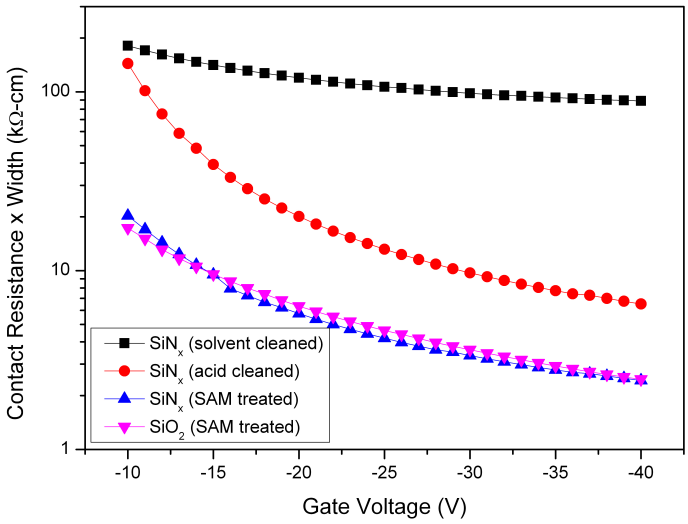


Figure 4.11: Contact resistance for pentacene TFTs on SiN_x substrates as a function of gate voltage

reported that a similar effect is brought about by UV-ozone treatment [78, 59], however, this step was only included in preparation for the SAM. It is thought that the presence of a thin oxide layer may in fact enhance the injection from contact metal to channel.

4.2 TFTs with 150 °C SiN_x Gate Dielectric

Having demonstrated the compatibility of pentacene with a PECVD SiN_x gate dielectric, it was decided to further investigate the applicability to real devices by studying the effect of the transition to a low temperature (150 °C) SiN_x. Furthermore, the effect on performance of material composition was studied. The materials development and properties have been described previously in section 3 for the SiN_x and section 4.1 for the pentacene.

4.2.1 Device Fabrication

While device fabrication followed a similar procedure to that discussed previously, a number of alternative self assembled monolayers were investigated, along with a more in depth consideration of cleaning procedures used and their effects upon the performance of devices. The dielectric layers investigated were:

Q2 SiO_2: thermally grown

C1 SiN_x: NH_3/SiH_4 40/2 (N-rich)

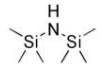
C2 SiN_x: NH_3/SiH_4 30/2

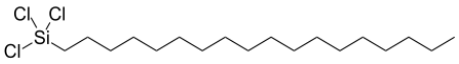
C3 SiN_x: NH_3/SiH_4 20/2

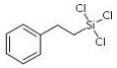
C4 SiN_x: NH_3/SiH_4 10/2 (Si-rich)

Each of these dielectric layers was treated in the same way, with identical post deposition processing steps. Initially photolithography was performed to allow for Ti/Au contacts to be defined. Following this each substrate was treated with the following process:

- Solvent clean,
- Piranha clean,
- UV/Ozone treatment, and then
- Self-asselmbled monolayer, either:

– Hexamethyldisiloxane (HMDS): 

– Octadecyltrichlorosilane (OTS): 

– β-phenethyltrichlorosilane (PHTS): 

To allow the fullest possible understanding of the action of each cleaning and processing step, a layer of pentacene was deposited on each of the substrates prepared in each of the steps discussed, yielding a matrix of thirty substrate and process combinations.

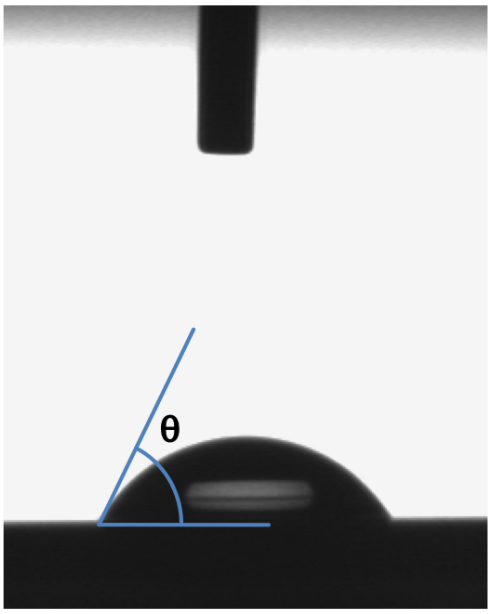
4.2.2 Device Characterisation and Parameter Extraction

A number of devices were examined at each process point, with TFT characteristics providing a useful materials analysis tool. However, before electrical characteristics were considered, the film microstructure was studied, enabling some understanding of the surface properties created by each cleaning/processing step, and also of the underlying properties of the various dielectric surfaces used.

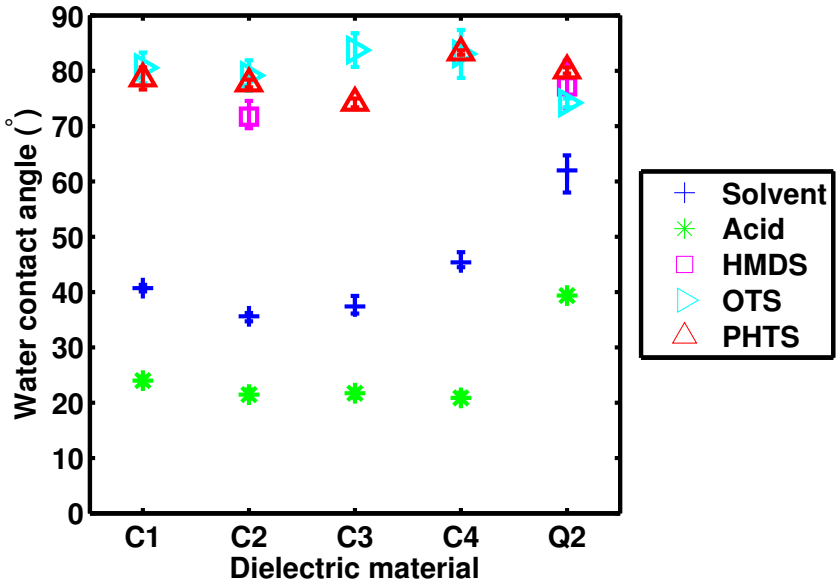
4.2.2.1 Surface characterisation

A brief study of surface condition was carried out before the deposition of any organic semiconductor, with water contact angle measurements used to compare each surface. Figure 4.12 shows the water contact angles measured for each of the process conditions used[1]. What is clearly evident is that PHTS and OTS significantly increase the water contact angle of all surfaces on to which they are applied, while HMDS has a lesser effect. However, piranha cleaned surfaces exhibit a far smaller water contact angle than those which have been solvent cleaned. These trends are to be expected, and can be explained by the fact that a piranha solution is highly oxidising, and will effectively oxidise the SiN_x/SiO_2 surfaces. The self-assembled monolayers, however, will bond to oxidised surface and present a non-polar interface at the surface, decreasing the surface energy and therefore increasing the water contact angle.

[1]Contact angle data is not available for UV/Ozone treated films, or for every substrate once it had been coated with HMDS.



(a) A water droplet on an acid cleaned SiO_2 surface.



(b) Contact angle measurements for a selection of surfaces

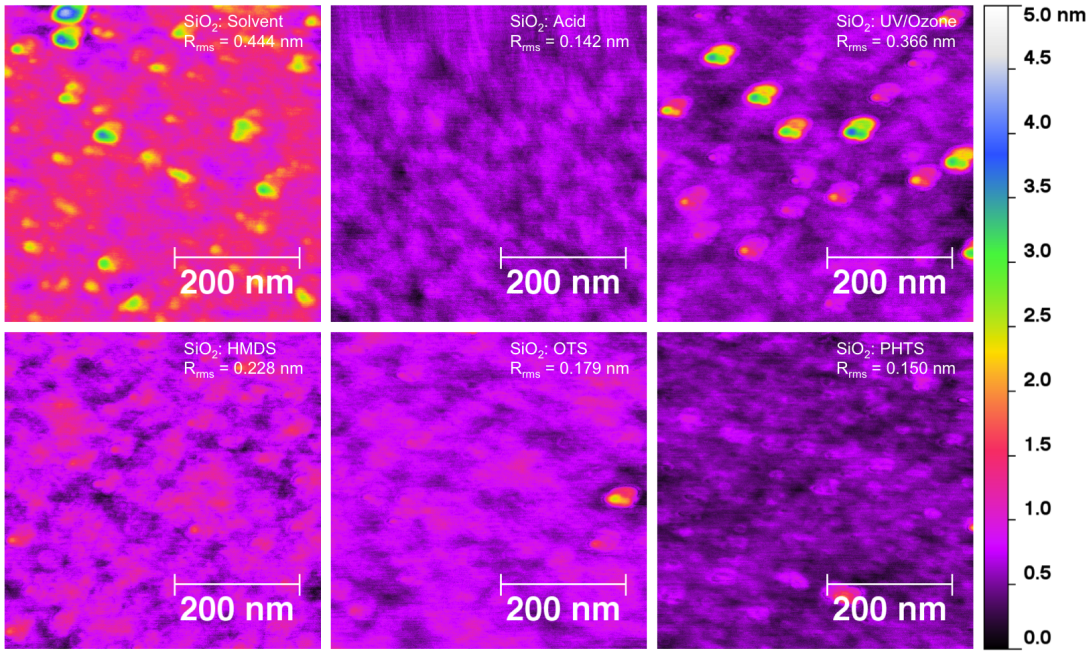
Figure 4.12: Contact angle measurements on several combinations of substrate and process. 'C1' etc. refer to dielectric, as defined in section 4.2.1.

Although specific data is not available in this work, several reports exist in the literature of UV/Ozone treatments being applied to Si/SiO_2 interfaces. For example, Baumgartner found that UV/Ozone treatment reduced the water contact angle of SiO_2 from 80 ° to approximately 3 ° [79]. Kitamura et al. found a similar treatment on SiO_2 surfaces resulting in a water contact angle of approximately zero degrees [80]. Furthermore, a similar treatment, that of an oxygen plasma, when applied to a SiN_x surface, has been shown to reduced the water contact angle to as low as 20 ° [81]. For the purposes of further qualitative analysis, the water contact angle of both SiN_x and SiO_2 treated with UV/ozone will be assumed to be 10 ± 10 ° .

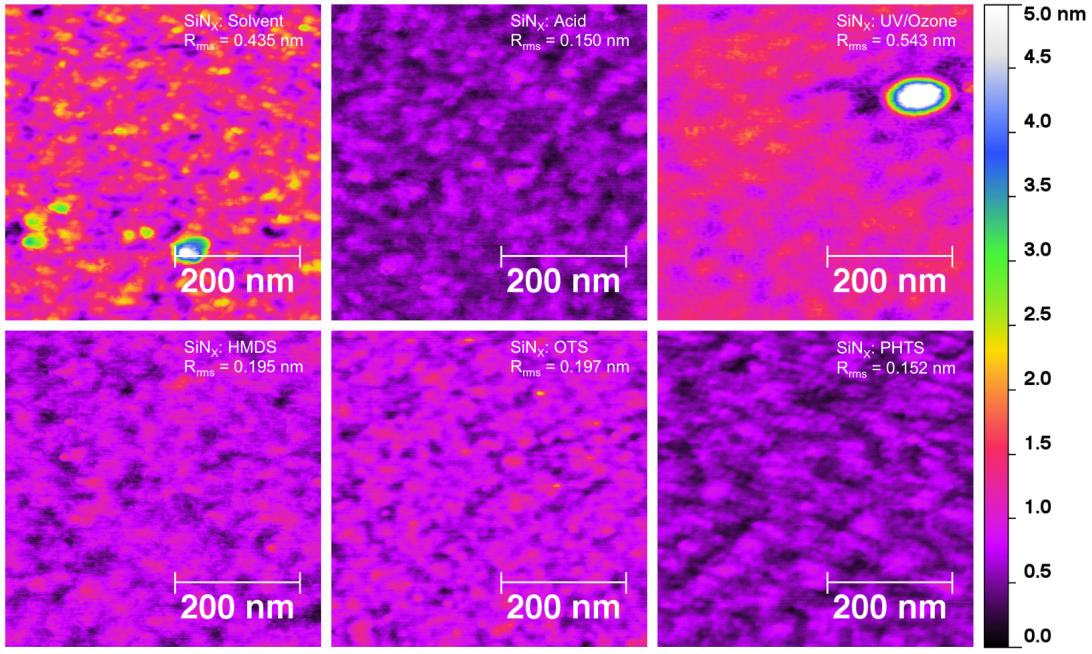
The intention behind using SAMs is to improve the surface condition ahead of the application of an organic semiconductor. In equivalent a-Si:H devices the dielectric/semiconductor interface can be prepared in high vacuum, with both materials (SiN_x/a-Si) deposited sequentially in one PECVD chamber, or at least without exposing the delicate surface to an ambient environment. This factor, along with the inherent compatibility between a-Si and SiN_x allows for an extremely high quality and low defect density interface to be prepared [82]. However, due to the constraints of device architecture dictated by the use of an organic semiconductor, it is not possible to use sequential dielectric and organic depositions, not least for the reason that metal contacts are required in advance of any organic deposition. A further complication is the intention to move from a simple common gate architecture to a more advanced integrated circuit architecture employing a discrete gate. For this reason, a dielectric surface, be it SiO_2 or SiN_x, will be exposed to an ambient atmosphere in advance of organic deposition, and will also have been subjected to a number of processing steps involved in photolithography, possibly resulting in a surface which is rather less clean than immediately after deposition. Furthermore, oxygen exposure is likely to have altered the surface chemistry somewhat.

The contact angle measurements displayed above support the expectation that the application of SAM layers will reduce the surface energy, as previously shown on SiO_2 surfaces [83]. This effect has also been demonstrated on SiN_x surfaces on several occasions [84].

The variously prepared surfaces were also examined by AFM, with an as-



(a) AFM images of treated SiO_2 surfaces.



(b) AFM images of treated SiN_x surfaces.

Figure 4.13: AFM images of variously treated SiO_2 and SiN_x surfaces. Each image is 500 nm × 500 nm.

sessment made of the surface roughness of each surface. Figure 4.13 shows the resultant AFM images taken of the SiO_2 (4.13a) and Si-rich SiN_x (4.13b) surfaces having been treated with each of the discussed processes. While any distinct features are hard to distinguish, the RMS roughness (R_{RMS}) values for each image allow a comparison to be made between each surface. While the SAM treated surfaces tend to have a smooth surface, with R_{RMS} <0.2 nm, the solvent cleaned and UV/Ozone treated surfaces tend to have surface roughness of >0.35 nm. A surprising result is that the acid cleaned surfaces, exhibit the smoothest of all treatments with a R_{RMS} of $\approx$ 0.15 nm for both SiO_2 and SiN_x. Most surprising though is that the UV/Ozone treatment tends to increase the surface roughness significantly, as the UV/Ozone treatment is always preceded by acid cleaning. Following this stage, which increases roughness, the substrates are then treated with one of the SAMs, with each of them once again reducing the roughness.

4.2.2.2 Film Microstructure

Having considered the surface properties of each substrate and treatment combination, AFM images of pentacene deposited on each surface were taken. These images are shown in figure 4.14, with each image representing a 10 $\mu m\times$ 10 μm region of pentacene.

Considering the collection of AFM images available a number of distinct trends are clearly visible. Surfaces treated with solvent cleaning only appear to have a small grain size, while surfaces which have been cleaned with an acid solution (piranha) exhibit the largest grain size of all, with some grains clearly spanning several μm in length. While a visual comparison of these images can be indicative of the pentacene morphology adopted under various conditions, only a qualitative assessment can be made. To allow a more thorough, quantitative analysis to be carried out some image and statistical analyses were carried out.

Each AFM image was subjected to a number of processing steps to detect grains, and then to create a mask corresponding to these grains. The image processing was performed by the use of the free tool Gwyddion [1], and the watershed grain detection algorithm [85]. Initially any deformation in the image plane is

[1] Gwyddion 2.20. http://gwyddion.net/

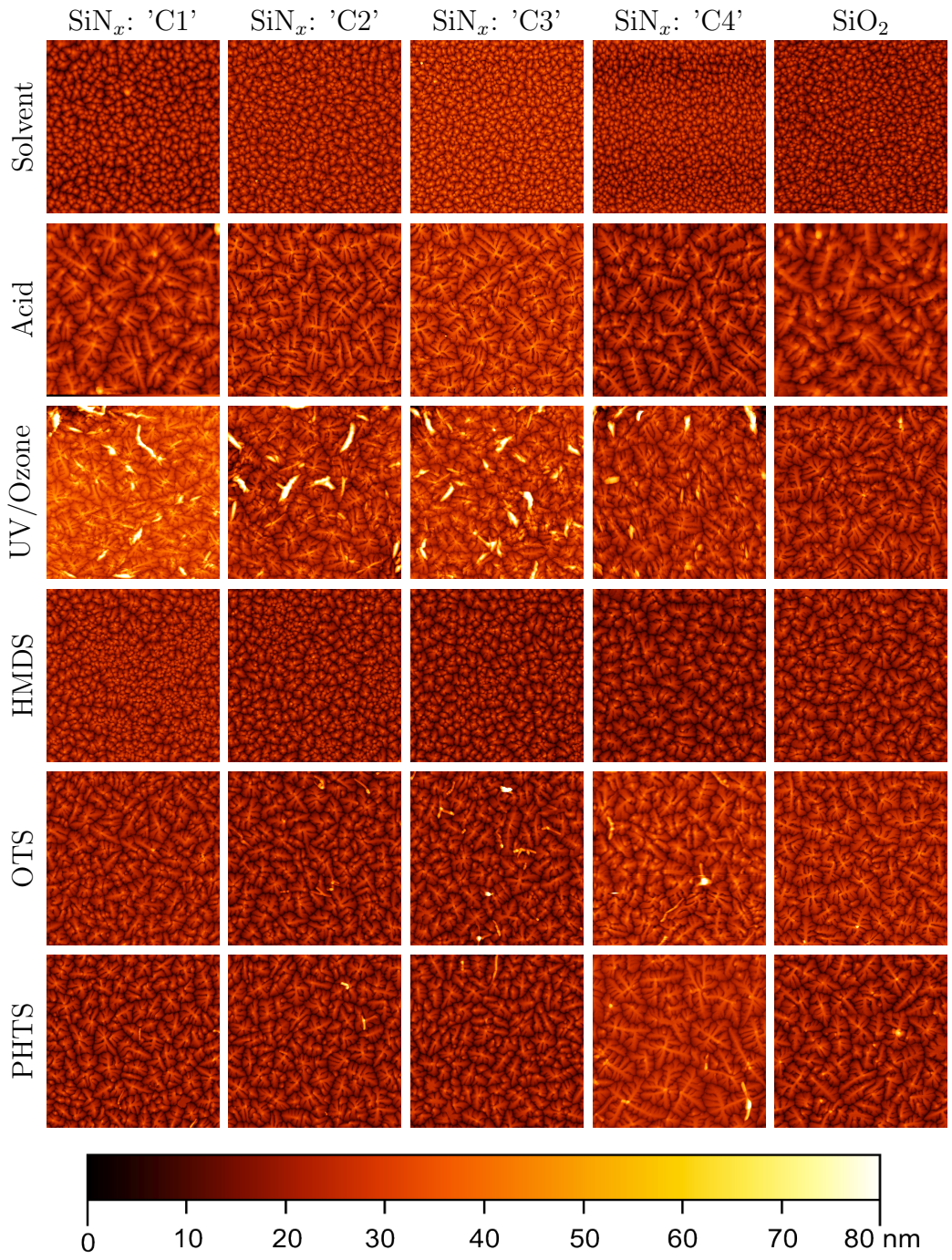
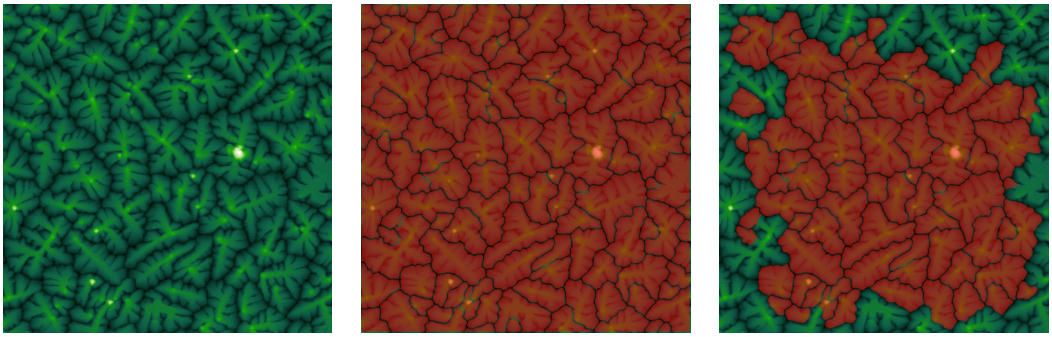


Figure 4.14: AFM images of pentacene on SiN_x with various surface treatments:solvent cleaned, acid cleaned, UV/ozone cleaned, HMDS treated, OTS treated and PHTS treated. All images 10 μm × 10 μm.



(a) AFM image **(b)** Grains detected **(c)** Edge grains removed

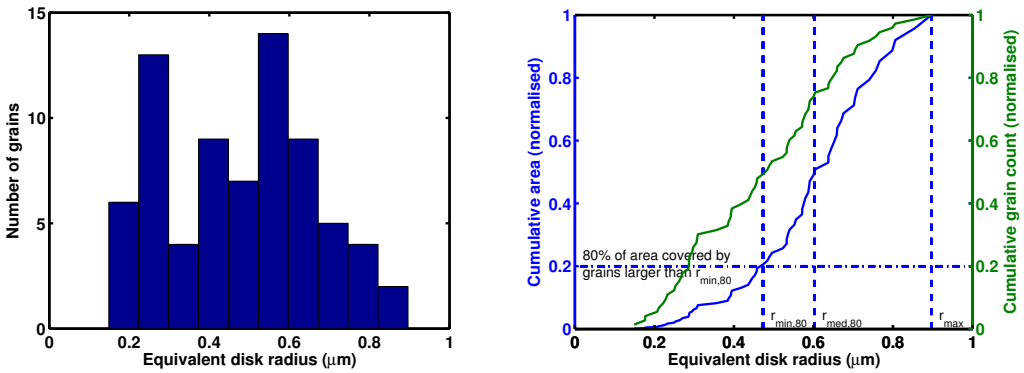
Figure 4.15: Grain detection and size analysis from AFM images. Example image used 5 $\mu m \times 5$ μm AFM image of pentacene on PHTS treated SiO_2 surface.

removed, by subtracting a fitted curved surface from the image intensities. The parameters used for the watershed algorithm were as follows:

Grain Location	Number of steps	3
	Drop size	13.11 %
	Threshold	42 px^2
Segmentation	Number of steps	200
	Drop size	5.01 %

With the parameters established to find a compromise between sensitivity and accuracy. The 'threshold' of 42 square pixels is the minimum grain size allowable, and corresponds to a grain of 0.00016 μm^2. This excluded any imaging defects from appearing as grains.

An illustration of this process is shown in figure 4.15, with the flattened AFM image shown in figure 4.15a. The extracted mask is shown in figure 4.15b. However, by inspecting this image it is apparent that many grains span the edges of the image, and as such, are not fully contained within the image. If the size of grains is to be studied, these grains will skew the sizes extracted as they will each be considered as whole grains. To compensate for this error, all grains which span the edges of each image were excluded from our analysis, as shown in figure 4.15c.



(a) Histogram of grain size distribution

(b) Cumulative grain area

Figure 4.16: Grain size distribution for pentacene on PHTS treated SiO_2 surface.

Once this processing step has been carried out for each image, a distribution of grain sizes is acquired. To allow a straight forward comparison to be made between grains of various shapes and sizes, the data is normalised to assume that each grain is a circular disk, with the single metric which describes each grain being the radius of that equivalent disk, R_{eq}. This parameter now has a distribution of lengths. Figure 4.16a shows a histogram of the distribution of grain sizes for the example image shown. Similar distributions can be observed for each image processed.

Further to this, to allow a comparison to be made between each process and material combination, it was considered necessary to extract a single representative length which best described the grain distribution. It will be appreciated that were this to be chosen as a numerical average, then it may be swayed by a large number of relatively small grains which do not in fact contribute to conduction. In fact, to aid understanding of this distribution the normalised cumulative area distribution is plotted as figure 4.16b. This plot demonstrates the insignificance of the large number of small grains, when compared to the relatively small number of larger grains. This effect will be appreciated by considering the images of figure 4.15. A further measure of disk radius was now considered, by reference to the cumulative normalised area, by considering the disk radius above which a certain percentage of the image area was covered. For example, disks with an equivalent radius of 0.72 μm or greater cover 50% of the total area, and as such

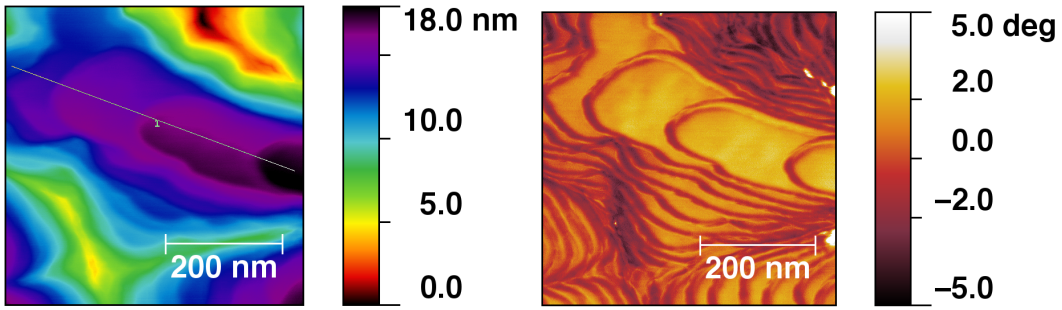
Surface Treatment	Substrate				
	SiN_x: 'C1'	SiN_x: 'C2'	SiN_x: 'C3'	SiN_x: 'C4'	SiO_2
Solvent	0.25	0.25	0.29	0.19	0.22
Piranha	0.78	0.63	0.64	0.71	0.76
UV/Ozone	0.49	0.56	0.48	0.44	0.58
HMDS	0.21	0.26	0.26	0.45	0.43
OTS	0.38	0.49	0.61	0.56	0.65
PHTS	0.47	0.52	0.44	0.99	0.65

Table 4.3: Median equivalent disk radius of largest grains covering 80 % of sample surface, $R_{med,80}$ (μm).

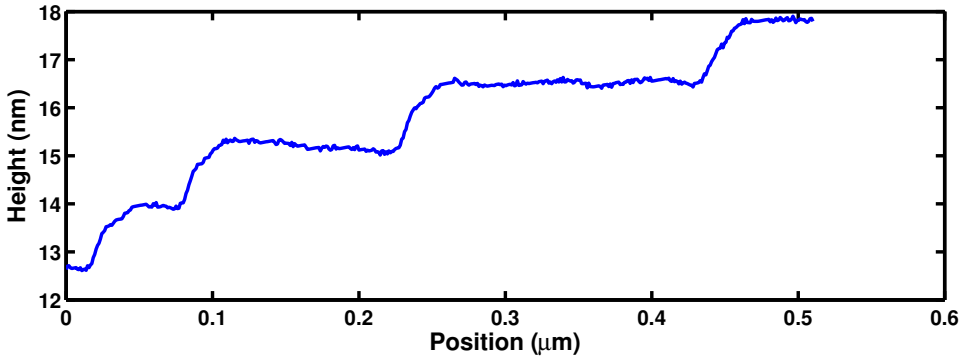
this radius can be described as $R_{min,50}$. The relationship between disk radius and cumulative area can be seen in figure 4.16b, which also shows the cumulative number of grains (in green).

The challenge with selecting the correct representative disk radius is to ensure that a (significant) majority of the current path through the organic thin film is captured by the measure used. An average grain size representing those grains contributing to conduction is required. As such the smallest 20% of grain are excluded, with a value of 80% coverage used. That is to say that an equivalent disk radius, $R_{min,80}$, is defined as the minimum equivalent radius of grains which make up 80% of the channel area. For comparison, the cumulative number of grains is also considered. The cumulative number of grains above a radius is clearly a misleading value, as the same radius would only account for 51% of the number of grains. Or, put another way, 51 % of the number of grains cover 80% of the device area in this device.

As discussed above, and to allow for a more useful comparison, an average value was sought, with the median disk radius of all of grains making up 80 % coverage ($R_{med,80}$) being used. In the case of the example illustrated, for pentacene on PHTS treated SiO_2, $R_{med,80} = 0.65$ μm. $R_{med,80}$ values for all pentacene films are shown in table 4.3. A significant degree of variation in grain size is clear here, as previously illustrated in figure 4.14. Characteristic grain radii vary from as low as 0.19 μm for a solvent cleaned SiN_x surface to as high as 0.99 μm for a similar surface treated with PHTS. It must also be noted that



(a) Height data **(b)** Phase data

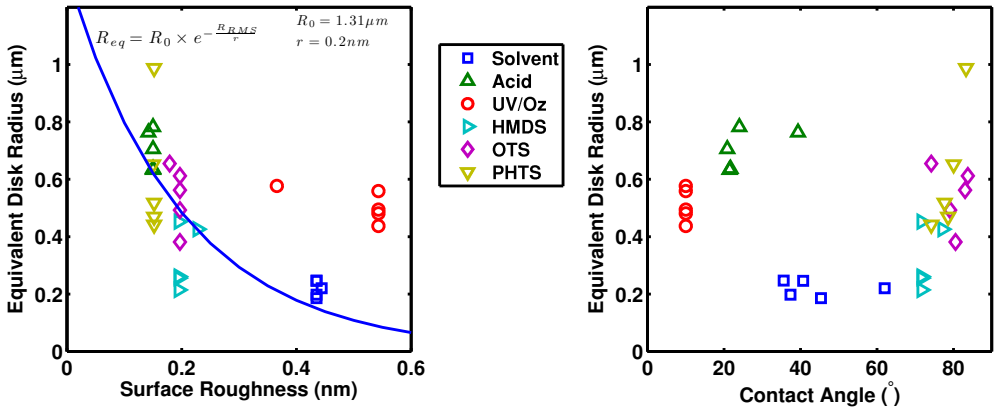


(c) Height profile scan

Figure 4.17: High resolution AFM image (500 nm × 500 nm) of pentacene on PHTS treated SiN_x, including height profile and phase image.

these numbers refer to disk radius, and as such, they should be doubled if an effective average grain length is to be considered.

Higher resolution AFM images can reveal further detail of the grain structure in some cases, with molecular terraces becoming visible. Figure 4.17a shows an AFM image of pentacene on PHTS coated SiN_x, with clear levels visible. The height profile of the line marked as '1' is shown in figure 4.17c, showing clear steps of ≈1.3 nm in height between each pentacene terrace. The phase image in 4.17b further illustrates the degree to which the pentacene surface is made up of a series of terraces. What becomes immediately apparent in this sample, is that during deposition grains must grow at a slow rate, with a high degree of molecular mobility of pentacene molecules incident upon the surface. A molecule



(a) Effect of surface roughness on grain size

(b) Effect of contact angle on grain size

Figure 4.18: Relationships between surface properties and pentacene grain size.

must travel a large distance (≈100s of nm) to find the next terrace edge, which is where it will preferentially be deposited.

While this image is taken from a device with relatively large grains, a similar terrace pattern is observable on all samples when examined closely. However, in samples with small grain sizes, terrace edges become closely spaced so as to appear continuous in some instances. It will be understood that a crucial point during the growth of pentacene grains is that of nucleation. Once a grain has begun to grow, it will provide a site to which subsequent molecules can join. Until this nucleation has occurred, incident molecules will search for a suitable low energy configuration which to adopt. Where a rough or high energy surface is present, as in the case of solvent cleaned surfaces, many such sites exist, and small grains will be the result. However, where a smooth and low energy surface is presented to the incident pentacene molecules, they must travel further to find an energetically suitable site, resulting in the formation of the large grains observed in figure 4.17.

Figure 4.18 allows us to examine the relationships between surface preparation techniques and subsequent pentacene grain sizes observed on each surface. While a significant degree of variation is visible in each set of measurements, a trend is visible linking grain size to surface roughness. Figure 4.18a shows this relationship, which appears to follow an approximately exponential function, provided

the contribution from surfaces treated with UV/Ozone is ignored. For all other devices, however, the following equation can be used to describe an approximate empirical relationship between the measured surface roughness and the observed pentacene grain size:

$$R_{eq} = R_0 \times e^{-\frac{R_{RMS}}{r}} \tag{4.1}$$

where R_{eq} is the equivalent disk radius, R_{RMS} the root mean square surface roughness and R_0 and r fitting parameters, which in this case are 1.31 μm and 0.2 nm respectively. While the line plotted does not exactly describe the relationship seen, it can prove a useful guide and tool for understanding the processes involved. R_0 can be thought of as an equivalent disk radius which might be observed in a perfectly smooth surface, while r is a roughness parameter which dictates the extent to which new grains nucleate upon a sub-optimal surface.

However, the fact that UV treated surfaces do no obey such a rule requires further consideration. Moreover, when surface energy is considered, it becomes apparent the that roughness model cannot describe the situation fully. Considering now figure 4.18b, a less clear picture is presented.

Several studies have previously probed the growth and nucleation of pentacene deposited by OMBD, with various growth models suggested [86]. In a report by Stabloder et al. the effect of surface roughness of various growth substrates is discussed, with a suggestion that grain area, A, is proportional to $\approx 1/R_{RMS}$ [87]. However, it is also noted that the surface energy may influence the growth mechanism significantly. Yang et al. considered the growth of pentacene on three substrates with different surface energies, as indicated by water contact angles ranging from 68 to 97 degrees [88]. Also in that work, it was shown that the larger water contact angle, corresponding to the lowest surface energy, led to the largest pentacene grain sizes. In that work, the effect of surface roughness was minimised by the use of similarly rough surfaces (R_{RMS} 0.31-0.37 nm, equivalent to some of of the rougher surfaces in our study). Heringdorf et al. showed that large pentacene grains approaching 100s of μm in size were achievable given the right surface and growth conditions, and relying on the ability to suppress grain nucleation sufficiently to allow a small number of grains to cover a large area [89].

Preparation of pentacene thin films on both hydrophobic dielectrics (PVP) and a more hydrophilic surface (SiO_2) was demonstrated by Mun et al. [27], where, like in Yang's work, a surface roughness of ≈0.3 nm was observed for both dielectrics. In this case it was suggested that large initial grain sizes on hydrophilic surfaces were replaced as film thickness increased with smaller grains, whereas for a low energy (hydrophobic) surface, such as PVP, smaller grains are observed. This observation is not widely reported, yet tends to agree with some results shown in this study.

While on the whole it appears that surface roughness dominates in determining grain nucleation density, surface energy may also contribute. Figure 4.18b demonstrates this fact, with some positive correlation clear between contact angle and grain size for solvent cleaned and SAM treated surfaces. However, in our study, all extremely hydrophilic surfaces, those with the highest surface energy, demonstrate enhanced grain size over the neutral (solvent cleaned) surfaces. In fact, on average, the treatment which brought about the largest grain size across all substrates (SiN_x and SiO_2) was acid cleaning. This suggests that Mun's view may be correct, and that the higher surface energy does in fact promote large crystal growth. However, this cannot be reconciled with the fact that both high and low surface energy surfaces lead to similar grain sizes. Rather, it is suggested that the presence of nucleation sites dominates the growth dynamic, except in the case of UV treated surface, where the extremely high energy surface can lead to incident pentacene molecules being driven to form larger grains in preference to forming new grains at any of the abundant nucleation sites provided by the comparatively rough surface.

Further consideration will be given to the contribution of surface roughness and surface energy to growth dynamics when devices have been examined electrically, as the electronic transport properties at the semiconductor-dielectric interface provide further evidence of molecular arrangement.

4.2.2.3 Electrical Characterisation

As with pentacene devices deposited on a higher temperature SiN_x substrate, all devices were electrically tested in a vacuum probe station, providing a stable en-

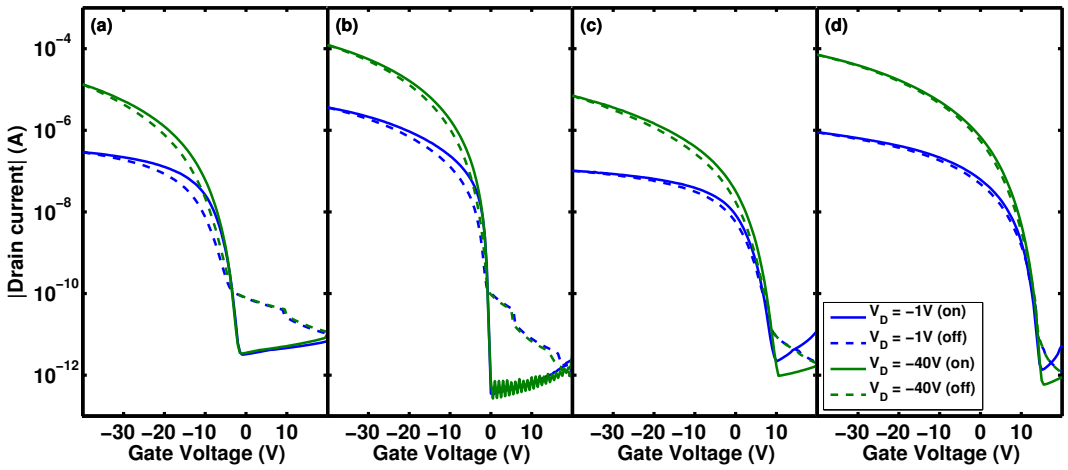


Figure 4.19: Transfer curves of pentacene TFTs on (a) SiN_x 'C4' with solvent cleaning, (b) SiN_x 'C4' with PHTS SAM, (c) SiO_2 with solvent cleaning and (d) SiO_2 with PHTS SAM. W=25 μm, W=500 μm. 'On' and 'off' refer to measurement direction.

vironment in which to study many devices. While air stability will be considered, devices were initially tested solely in vacuum, so that each of the 100+ devices probed would have been exposed to ambient conditions for a similar duration. Each test was run with the same 'normal' speed settings using Keithley 5200 SCS.

As can be seen from illustrative examples of TFT transfer curves shown in figure 4.19, there is a large degree of variation in the 'on' current between devices with different preparation treatments. Figure 4.19 (a) and (c) relate to device which have been solvent cleaned, while (b) and (d) show devices treated with PHTS SAM. Approximately an order of magnitude increase in current can be seen between the solvent cleaned and PHTS treated devices. While results shown are for one channel length only ($25\mu m$), and for SiO_2 and SiN_x C4 substrates, they are representative of the distribution of results seen.

Output characteristics of the same devices are shown in figure 4.20, with the vertical axis for parts (a) and (c) stretched to allow the behaviour of the devices to be seen. Again an order of magnitude increase in current is seen as a result of the PHTS SAM surface treatment. The small degree of hysteresis during measurements can be observed from these data. These results also correlate well

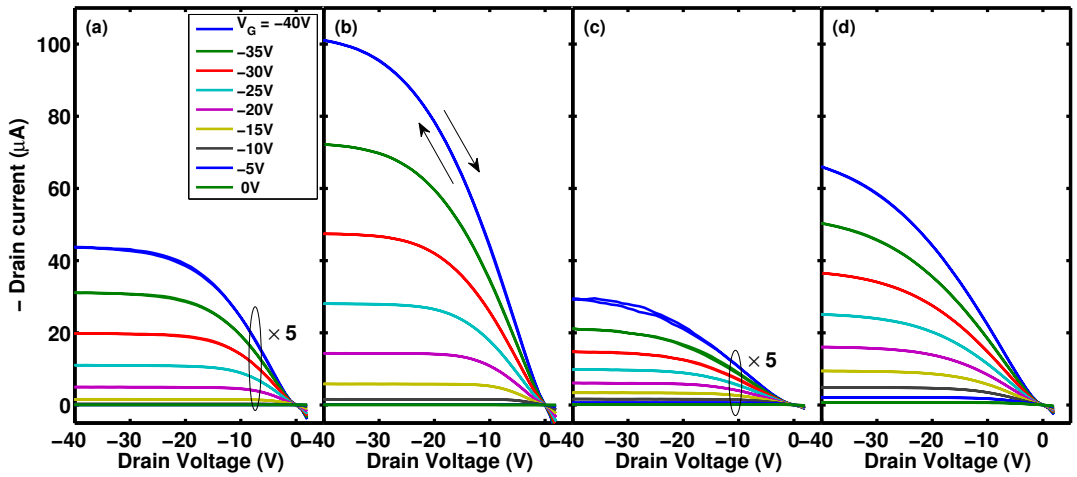


Figure 4.20: Output curves of pentacene TFTs on (a) SiN_x 'C4' with solvent cleaning (multiplied by 5), (b) SiN_x 'C4' with PHTS SAM, (c) SiO_2 with solvent cleaning (multiplied by 5) and (d) SiO_2 with PHTS SAM. W=25 μm, W=500 μm.

with behaviour seen previously while using a SiN_x dielectric deposited at 300 °C.

Measurements were made on devices of six channel lengths for each of five test substrates and six surface conditions, yielding 180 combinations. The data collected from this large number of devices was analysed to allow a number of TFT characteristic parameters to be extracted. The degree of correlation between this large number of data points allows some confidence in the average values extracted, and provides a far fuller illustration of device behaviour than the preliminary studies carried out previously. Furthermore, an assessment can be made of the suitability of each set of devices for their use in large area application requiring a high degree of consistency and repeatability.

4.2.2.4 Parameter Extraction

While standard analysis techniques are available to extract useful TFT parameters such as field effect mobility, threshold voltage, sub-threshold slope, on-off ratio and contact resistance (see section 2.3.1), it is worth considering also their limitations. Furthermore, while allowing for non-idealalities in parameter extraction technique, non-idealities in materials and interfaces can also interfere with the precise interpretation of collected data. For example, considering the plots

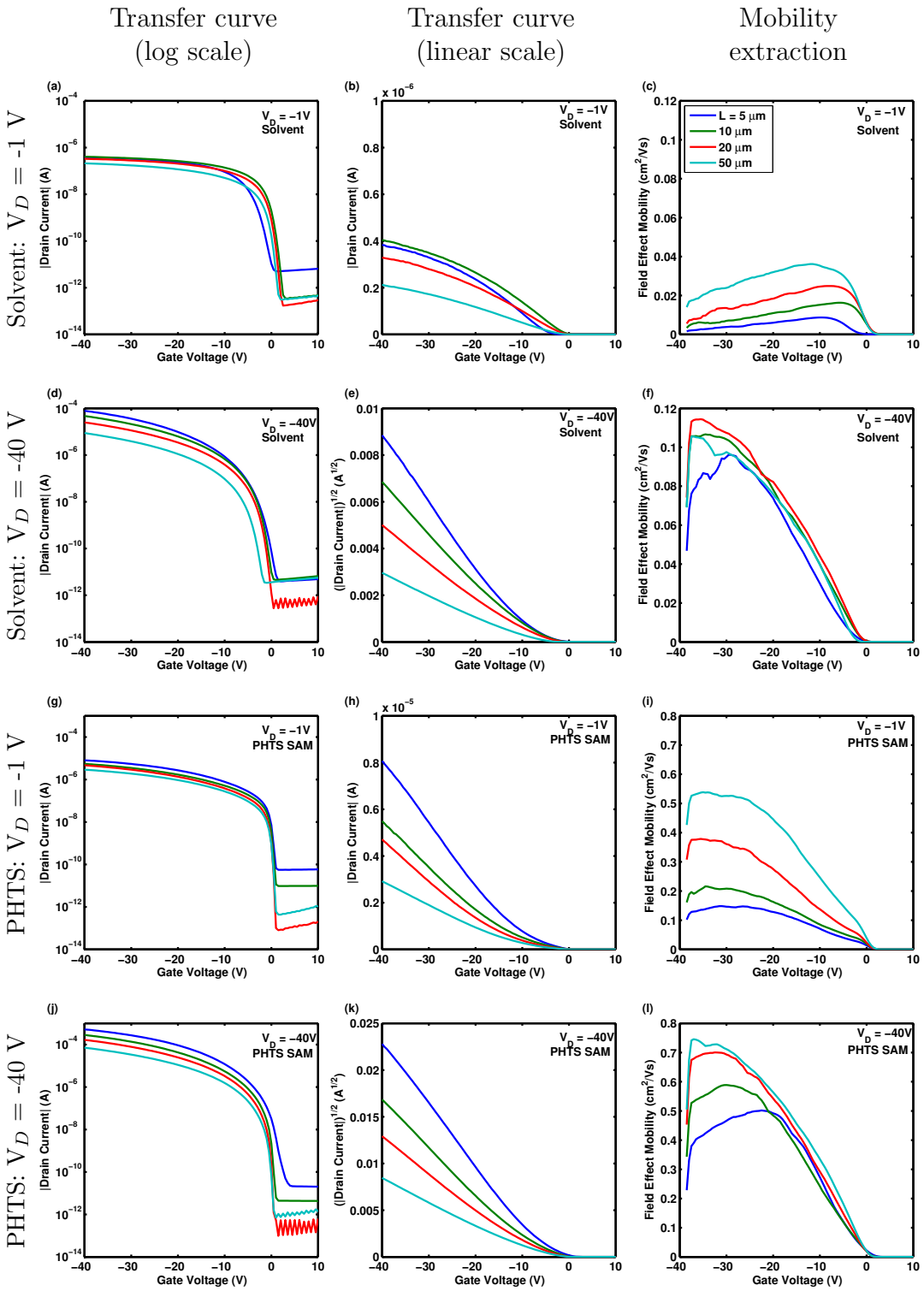


Figure 4.21: Device non-idealities leading to errors in parameter extraction from pentacene TFT measurements: transfer curves and field effect mobility extraction for pentacene TFTs on Si-rich SiN$_x$ ('C4'), with solvent cleaned and PHTS SAM treated surfaces, using channel lengths of 5, 10, 20 and 50 μm, measured in the linear (V$_D$ = -1V) and saturation (V$_D$ = -40V) regimes.

shown in figure 4.21, which shows the extracted field effect mobility for a selection of pentacene TFTs on Si-rich SiN_x. The corresponding transfer curves are also shown, both on a logarithmic scale and a linear scale. What is immediately apparent is the change in form of each mobility curve.

For a TFT based on a solvent treated surface, and biased in the linear regime (figure 4.21 parts a-c), there is a clear mobility maximum at $\approx$ -10 $\pm$ 5 V, close to the threshold voltage for that device. However, for the same device biased in the saturation regime(figure 4.21 parts d-f), the field effect mobility appears to increase throughout the extent of the measurement range, with a maximum appearing close to -40 V or possibly beyond (figure 4.21 (f)). This phenomenon can be understood with reference to the corresponding transfer curves, when plotted on a linear scale. A comparison of figures 4.21 (b) and (e) show that towards the maximum applied voltage (-40 V) the device in the linear regime (b) shows a pronounced decrease in rate of increase. However, in the saturation regime (e) this effect cannot be observed, with a constant rate of increase seen across the range. It will be seen that this decrease in rate is responsible for the apparent reduction in mobility, but is itself likely to be caused by the significant injection barrier at the contact-semiconductor interface.

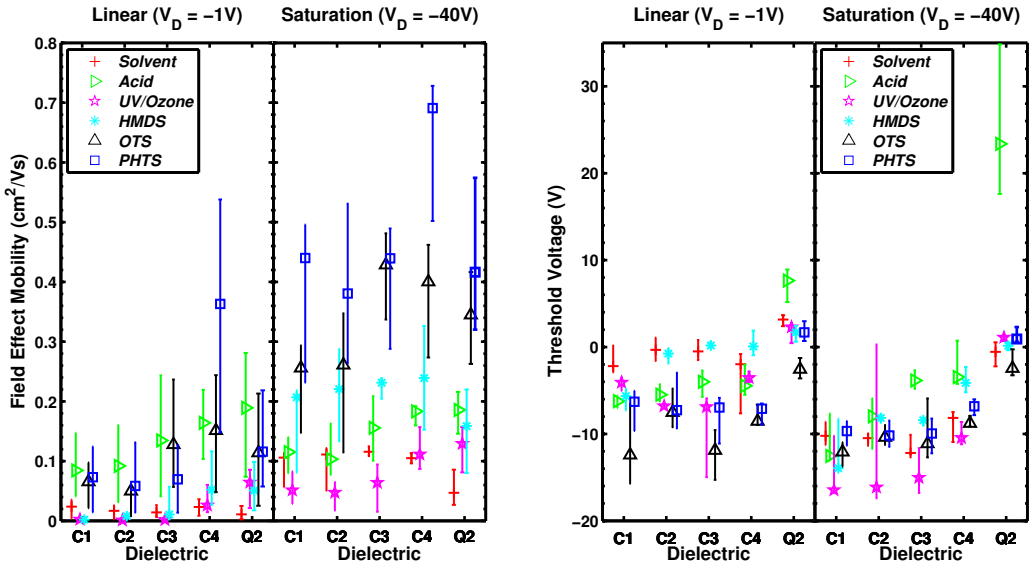
It can also be seen that a device's channel length has a significant effect on the extracted mobility. In fact, for the devices shown in figure 4.21 (c), the extracted mobility will vary from as low as 0.01 cm^2/Vs for a 5 μm length device, to almost 0.04 cm^2/Vs for a 50 μm length device. However, the same devices biased in the saturation regime show more consistent mobilities of $\approx$ 0.1 cm^2/Vs, a marked increased.

Now considering the similar plots shown in figures 4.21 (g)-(i) where a PHTS SAM was applied, it can be seen that the mobility curves appear to saturate at a more stable value for each length, while there is still a significant variation between devices of each channel length. Figures 4.21 (j)-(l) complete the set of plots, with devices also having SAM treatment, but now biased in the saturation regime. Here there is a further increase in mobility and, on the whole, good agreement between devices of different channel lengths, suggesting a reduced injection barrier.

It is with the above discussed limitations in mind that we consider figure

Substrate	Surface Treatment	Mobility μ (cm^2/Vs)		Threshold Voltage V_T (V)		Sub-threshold Slope SS $(V/decade)$		Hysteresis H (V)		Contact Resistance R_C $(k\Omega - cm)$
	V_D (V)	-1	-40	-1	-40	-1	-40	-1	-40	-1
SiN_x: 'C1'	Solvent	0.024	0.106	-2.2	-10.2	0.34	0.67	8.2	3.0	196.0
	Acid	0.084	0.115	-6.2	-12.5	0.33	0.97	13.8	5.0	21.2
	UV/Ozone	0.002	0.051	-4.1	-16.5	0.46	8.46	15.0	5.8	1304.6
	HMDS	0.002	0.207	-5.6	-13.9	0.21	0.32	6.0	3.5	2351.6
	OTS	0.065	0.256	-12.4	-12.1	0.26	0.40	7.2	4.0	14.1
	PHTS	0.073	0.440	-6.3	-9.7	0.19	0.28	5.8	2.2	77.8
SiN_x: 'C2'	Solvent	0.017	0.111	-0.3	-10.5	0.32	0.50	10.0	3.8	330.4
	Acid	0.092	0.103	-5.5	-8.0	0.84	0.76	12.5	5.2	22.5
	UV/Ozone	0.001	0.047	-6.8	-16.1	1.75	7.73	14.2	6.5	3123.5
	HMDS	0.006	0.211	-0.8	-8.4	0.36	3.47	7.0	4.0	383.5
	OTS	0.050	0.261	-7.5	-10.4	0.23	0.34	8.2	4.0	80.8
	PHTS	0.058	0.380	-7.3	-10.2	0.18	0.37	6.0	2.5	130.7
SiN_x: 'C3'	Solvent	0.014	0.116	-0.5	-12.2	0.43	0.54	11.5	4.0	309.2
	Acid	0.134	0.156	-4.0	-3.8	1.27	1.41	7.5	4.0	18.1
	UV/Ozone	0.002	0.064	-6.9	-15.0	1.26	10.23	11.0	5.8	2636.1
	HMDS	0.008	0.225	0.4	-8.4	0.23	0.32	10.0	4.5	725.6
	OTS	0.128	0.428	-11.9	-11.1	0.33	0.45	7.0	3.5	16.2
	PHTS	0.069	0.439	-7.0	-9.9	0.21	0.26	5.8	2.0	73.7
SiN_x: 'C4'	Solvent	0.023	0.105	-2.0	-8.2	0.54	0.79	4.8	2.0	105.9
	Acid	0.172	0.184	-4.9	-3.6	1.42	1.27	4.0	2.5	4.0
	UV/Ozone	0.026	0.111	-3.5	-10.4	0.87	6.38	10.8	4.0	82.1
	HMDS	0.052	0.239	0.1	-4.1	0.32	0.31	5.8	3.5	74.3
	OTS	0.151	0.400	-8.5	-8.8	0.20	0.31	7.0	3.8	23.3
	PHTS	0.363	0.691	-7.1	-6.8	0.28	0.32	2.5	1.2	6.4
SiO_2: 'Q2'	Solvent	0.011	0.047	3.2	-0.6	1.50	1.25	1.0	1.8	600.3
	Acid	0.189	0.186	7.7	23.4	14.79	12.25	1.5	1.0	15.2
	UV/Ozone	0.064	0.129	2.3	1.1	2.60	8.96	6.5	3.2	42.1
	HMDS	0.051	0.159	1.7	0.2	0.66	0.57	2.0	2.0	76.1
	OTS	0.114	0.345	-2.6	-2.4	1.05	0.71	2.0	1.0	73.2
	PHTS	0.116	0.416	1.7	0.9	1.06	0.81	1.5	0.5	32.7

Table 4.4: Pentacene TFT parameter summary for each surface and treatment combination. Median values presented for each combination, considering devices of 6 channel lengths (5, 10, 15, 20, 25 and 50 μm).

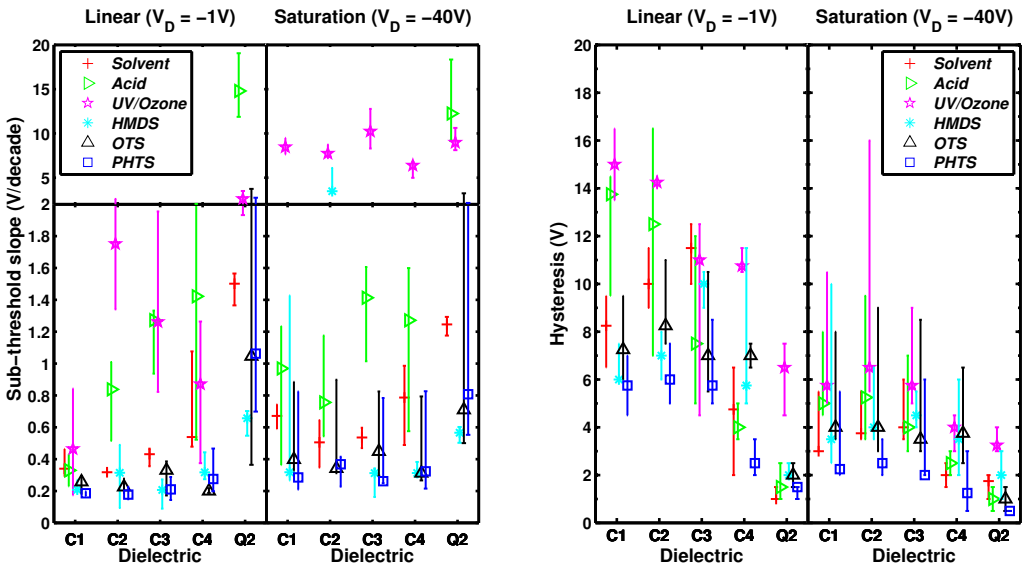


(a) Field effect mobility distribution

(b) Threshold voltage distribution

Figure 4.22: Distribution of extracted TFT parameters for pentacene devices on various substrates and with various substrate treatments. 'C1' etc refer to dielectric, as defined in section 4.2.1.

4.22, which shows a summary of threshold voltage and mobility as extracted from electrical measurements of pentacene TFTs. A complete summary of TFT parameters is shown in table 4.4. What is immediately clear from figure 4.22 is the discrepancy between mobility values extracted in the linear regime and the saturation regime. As previously discussed, these values should be equivalent, and can be extracted using equations 2.1 and 2.2 respectively. It is worth considering these values while also looking at figure 4.20. It will be appreciated that in the low V$_D$ region (0V $>V_D >$-5V) the drain current appears to be slightly suppressed. In an ideal device, in the this region of operation, the I_D-V_D characteristic will exhibit a linear relationship, obeying Ohm's law. However, in the case where the contact resistance is large in comparison to channel resistance, then channel current at small operating voltages will be suppressed. Alternatively, at high V_D values ($V_D <$-20V), there is no-longer an expected linear relationship, and drain current should no-longer depend on drain voltage (provided it is greater than $V_G - V_T$). For this reason, and where a high contact resistance is seen, field effect



(a) Sub-threshold slope distribution

(b) Hysteresis distribution

Figure 4.23: Distribution of extracted TFT parameters for pentacene devices on various substrates and with various substrate treatments. 'C1' etc refer to dielectric, as defined in section 4.2.1.

mobility will be extracted in the saturation regime, according to equation 2.6.

Now we will briefly consider another important TFT parameter: sub-threshold slope. This is extracted by considering the maximum slope in the turn on region just below threshold voltage, as illustrated by figure 2.4a. One issue with such a measurement is the relatively large gate voltage measurement sampling step size of 0.5 V means, which dictates that the sharpest turn-on region will be observed for just a few measurement points, and as such any measurement is susceptible to significant errors. It should be noted at this point that errors due to insufficient sampling resolution can only yield an under-estimate of true sub-threshold slope, as illustrated in figure 2.5.

However, bearing those limitations in mind once more, figure 4.23a shows the wide distribution of sub-threshold slope values extracted for each device. While there is a large degree of variation is the slope for acid and UV/ozone treated devices, the SAM coated substrates appear to have a low and stable slope.

A result of potential significance is also that the SiO_2 devices tend to have a

significantly higher SS than the SiN_x equivalent devices, a surprising result, but also consistent with results using a higher temperature SiN_x. It should be noted that the extremely high values seen for acid cleaned SiO_2 substrates is an artefact of the threshold voltage shift seen in those devices, which can be seen in figure 4.22b. For the measurement range considered (-40V − +20V) the devices do not fully turn off, and as such, the slope extracted is only the maximum slope seen in that range, and not the true sub-threshold slope.

Similarly, the UV/Ozone devices exhibit an significant 'off' current, which appears as an ohmic conduction path in parallel with the device channel. As such, at high drain voltage biases, a significant 'off' current flows, which tends to mask the sharp turn on characteristic of the device's channel.

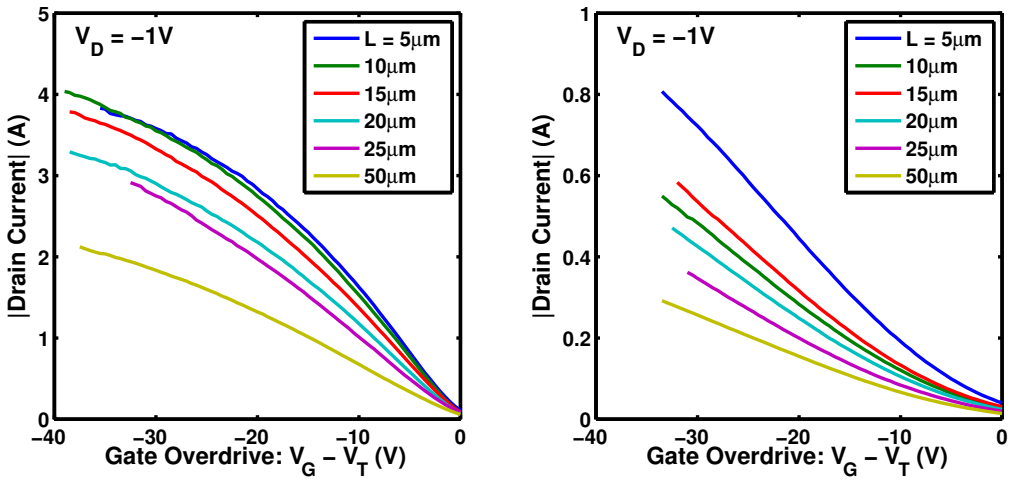
Now considering a further TFT parameter of interest: hysteresis. This was illustrated briefly in figures 4.19, where both the switch-on (solid), and switch-off (dashed) curves were plotted. To allow a good understanding of device behaviours a quantitative measure of hysteresis was required. This was devised as the difference in gate voltage between turn-on and turn-off when the drain current was 10% of its maximum, as illustrated in figure 2.7.

A summary of the hysteresis for each pentacene device is shown in figure 4.23b. As with the other device parameters, there is a significant degree of variation between each set of devices. Perhaps most significantly here is that the hysteresis in the linear regime is greater than that in the saturation regime. It would appear that more charge is being trapped under modest bias conditions than under more significant bias.

A secondary observation is that all devices fabricated on SiO_2 appear to have a small degree of hysteresis, suggesting that that material provides the most stable operating substrate.

Of the various surface treatments examined, the SAM treatments tend to reduce the hysteresis the most, with PHTS SAM proving, once again, that it provides an advantage over both OTS and HMDS.

As has been mentioned above, and discussed more thoroughly with reference to pentacene devices on a high temperature SiN_x substrate (4.1.2.3), contact resistance plays a significant roles in determining device performance. Without efficient carrier injection into organic materials it is impossible to utilize their



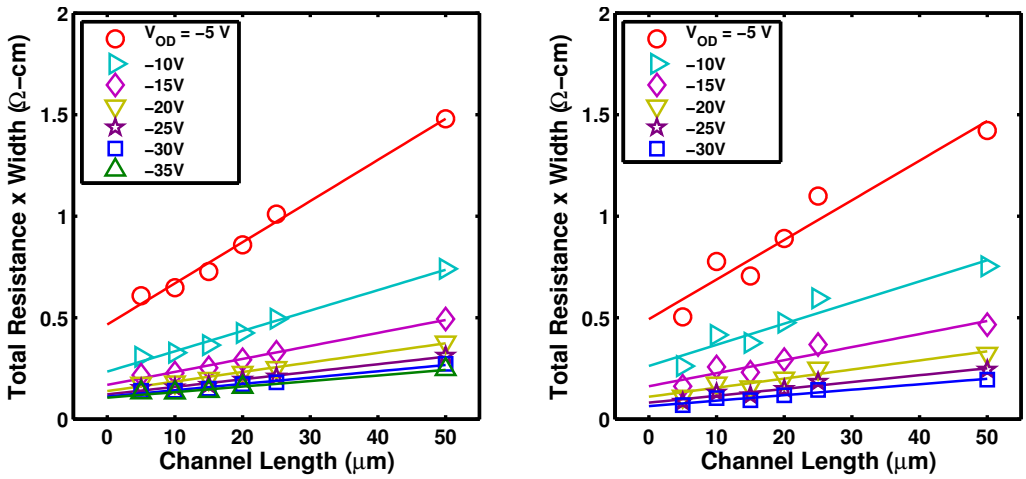
(a) Sovent cleaned SiN_x 'C4'. **(b)** PHTS treated SiN_x 'C4'.

Figure 4.24: Linear regime transfer curves for several lengths of pentacene TFT on SiN_x ('C4') with gate voltage normalised to threshold voltage.

current carrying properties. Having carried out extensive tests on a large number of devices, it has been possible to compile those test results to examine some characteristics of the materials and processes involved, without putting too much emphasis an any one individual experimental result.

Firstly, considering the plots of drain current against gate overdrive voltage (V_{OD} = V_G - V_T) for various channel lengths shown in figure 4.24 it will be appreciated that a variation in threshold voltage will limit the range of V_{OD} which can be used for comparison between devices. For the devices shown, it appears that for solvent cleaned devices (4.24a) there is a wider voltage range available than for PHTS treated devices (4.24b). A further observation which can be made from the comparison of solvent cleaned substrates to PHTS coated ones is that the solvent cleaned ones show a clear reduction in slope towards the maximum applied voltage.

Now considering 4.25, it can be seen that there is a high degree of correlation between the length of device and the total resistance for a particular gate overdrive voltage for both sets of devices illustrated. This characteristic varies from one process to another, with some poor devices leading to a distortion in some cases, but this can be minimised by excluding any devices whose transfer curve does



(a) Sovent cleaned SiN_x 'C4'. **(b)** PHTS treated SiN_x 'C4'.

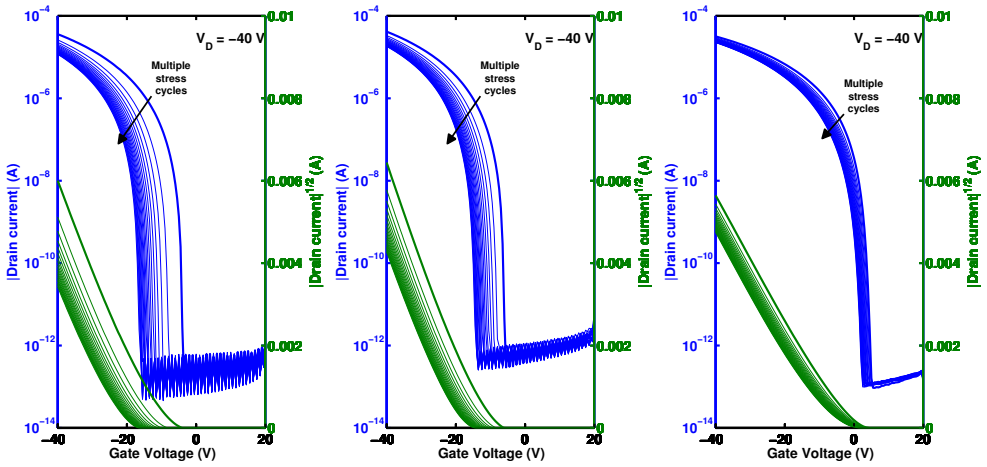
Figure 4.25: Total resistance versus length of pentacene TFT on SiN_x ('C4') at various gate overdrive voltages.

not have a standard form due to some defect or other.

In the case of the devices illustrated here, a clear offset can be seen where the apparent channel length is zero. This term can be equated to a zero-length resistance, or contact resistance, as described in section 2.3.1.4. As can be seen, this value reduces significantly as V_{OD} increases. The resulting minimum contact resistance value for each family of devices is shown in table 4.4.

4.2.2.5 Bias Stress Instability

Having examined a number of TFT parameters, a brief consideration will be given to their performance under continuous use. While isolated quasi-static measurements are useful in exploring parameters which are indicative of device behaviour, the fact that these measurements are not entirely repeatable or stable in some instances must not be neglected. There is extensive literature on the effects and origins of bias stress instability in thin film transistors, with a number of studies considering the use of a SiN_x dielectric [90], here applied to nc-Si:H TFTs for use in AMOLED displays. In that work, both interface and bulk effects are considered, while attention is also given the effect of SiN_x composition [91]. Investigations into the origins of bias stress instabilities of pentacene TFTs have



(a) SiN_x 'C1' **(b)** SiN_x 'C4' **(c)** SiO_2

Figure 4.26: Electrical characteristics of pentacene TFTs on PHTS treated SiN_x and SiO_2 surfaces after the application of bias stress. Stress conditions: V_G = -20 V, V_D = -1 V, Stress period = 1800 s, Stress cycles = 20.

suggested that the interface is crucial, while also highlighting the importance of the channel-contact interface in achieving stable device operation [25].

Figure 4.26 illustrates the effect of bias stress on both N and Si-rich SiN_x and SiO_2 based PHTS treated pentacene TFTs. In all measurements, a continuous gate bias stress of -20 V was applied, with a drain bias of -1 V. Transfer curve measurements were taken at intervals of 1800 seconds (30 minutes) in both the linear (V_D = -1 V) and saturation (V_D = -40 V) regimes of operation. Twenty stress cycles were performed on each device, with initial characteristics (bold lines) and each subsequent measurement (fine lines) displayed.

What is immediately apparent is the small change in characteristics of the SiO_2 based device when compared to either SiN_x devices, a slight shift in threshold voltage is visible in all cases, but with a varying degree. More subtle is the change in shift between N and Si-rich SiN_x devices, with the N-rich dielectric producing a larger shift than the Si-rich alternative. TFT parameters were extracted from each measurement for each device and are summarised in figure 4.27 and table 4.5 for both linear and saturation regimes. The magnitude of the field effect mobility measured in the linear regime should be disregarded, for reasons previously discussed, but its shift closely mirrors that in the saturation regime.

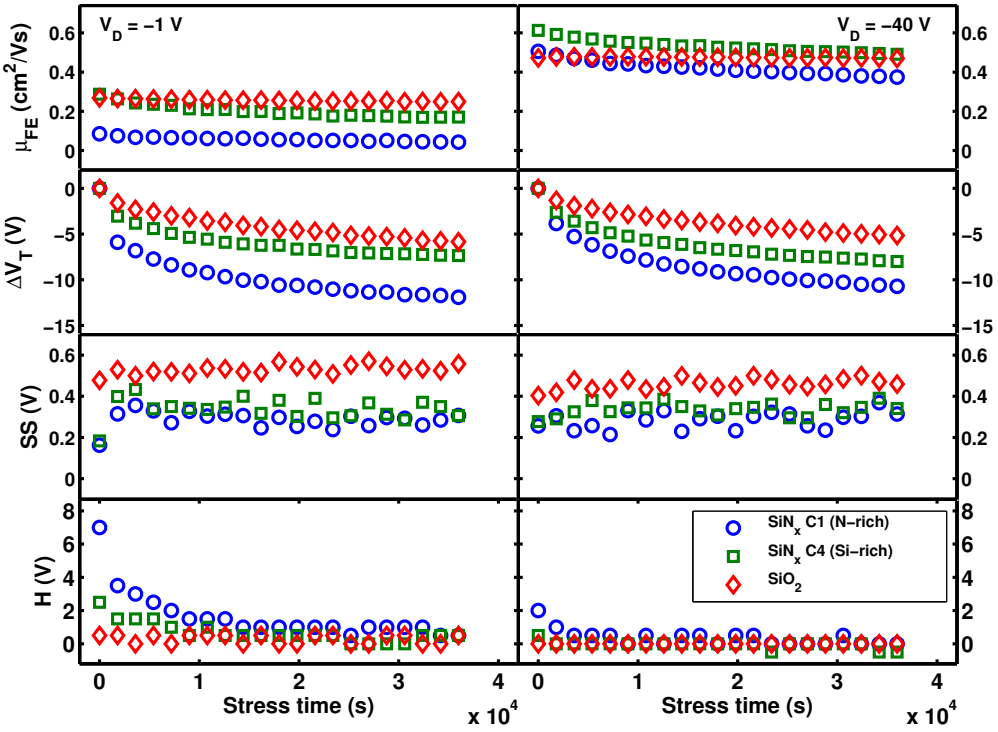


Figure 4.27: Summary of parameters of pentacene TFTs on PHTS treated SiN_x and SiO_2 surfaces after the application of bias stress. Stress conditions: V_G = -20 V, V_D = -1 V, Stress period = 1800 s, Stress cycles = 20.

The mobility observed in SiO_2 devices is extremely stable across the stress period. However, both compositions of SiN_x exhibit a reduction in mobility of approximately 20% during the stressing period. It is suggested that this reduction is not in fact due to any real reduction in field effect mobility, but is just an effect of the shift in threshold voltage, moving the maximum field effect mobililty outside the measurement range considered.

Most noticeable is the shift in V_T, with all characteristics showing some shift. The largest ΔV_T is seen in the N-rich SiN_x, with a shift in excess of 10 V. The most stable devices were based on SiO_2, with a shift of around 5 V towards the value of bias stress applied. Si-rich SiN_x showed a shift of between 7 and 8 volts, midway between the other devices considered.

Briefly considering the other parameters shown, we can see that a slight increase in sub-threshold slope can be seen in all devices during the measurement

Substrate	Cycle	Mobility μ (cm^2/Vs)		Threshold Voltage V_T (V)		Sub-threshold Slope SS $(V/decade)$		Hysteresis H (V)	
	V_D (V)	-1	-40	-1	-40	-1	-40	-1	-40
SiN_x 'C1'	t_0	0.085	0.506	-6.0	-10.6	0.16	0.26	7.0	2.0
	t_{20}	0.042	0.375	-17.9	-21.4	0.31	0.31	0.5	0.0
	Δ	-0.043	-0.131	-11.9	-10.7	0.14	0.06	-6.5	-2.0
SiN_x 'C4'	t_0	0.287	0.613	-10.7	-11.7	0.18	0.28	2.5	0.5
	t_{20}	0.170	0.491	-18.1	-19.7	0.31	0.34	0.5	-0.5
	Δ	-0.117	-0.122	-7.4	-8.0	0.12	0.06	-2.0	-1.0
SiO_2 'Q2'	t_0	0.268	0.473	-1.0	-2.0	0.48	0.40	0.5	0.0
	t_{20}	0.249	0.470	-6.9	-7.2	0.56	0.46	0.5	0.0
	Δ	-0.019	-0.003	-5.8	-5.2	0.08	0.06	0.0	0.0

Table 4.5: Electrical characteristics of pentacene TFTs on PHTS treated SiN_x and SiO_2 surfaces after the application of bias stress. Stress conditions: V_G = -20 V, V_D = -1 V, Stress period = 1800 s, Stress cycles = 20.

cycle. However, what is also apparent is the measurement noise which manifests as a variation between subsequent measurements of a significant proportion of the extracted values, reducing the significance any any observed changes.

Hysteresis is plotted for all devices too, with a marked reduction after a few measurement cycles for each of the SiN_x devices to a level which is no-longer detectable. This effect, along with the continuing shift in V_T for those devices suggests that there are multiple processes with differing time scales driving the shift in device performance.

In early work on pentacene TFTs Knipp et al. suggested that the pentacene material itself was the cause of bias stress instability, rather than the dielectric [16]. However, the results here tend to suggest that the picture is more complex than this, with some contribution likely from both components, plus the interface between the two.

Further work on this matter would be extremely beneficial, with a dynamic bias stress analysis likely to shed further light on the origins of bias stress insta-

bility, such as that performed by Miyadera et al. on SiO_2 based devices [92].

4.3 Discussion

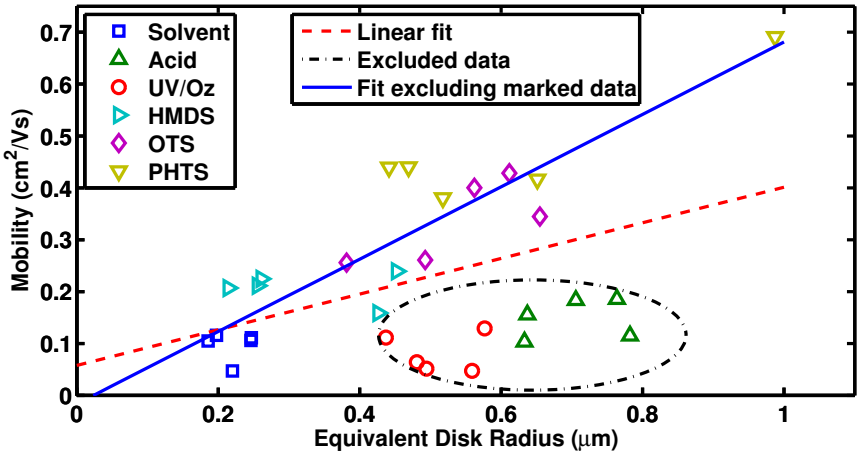
Having now considered a large number of devices and their performance under a variety of test conditions it is possible to reflect upon the data collected, and to examine the trends expressed therein. While a large degree of variability has been observed between supposedly similar devices, the large number of devices tested has reduced the reliance on any single result or device behaviour. We assess the effect of substrate surface condition and dielectric composition on device performance, and also discuss the effect of device preparation on contact resistance.

4.3.1 Surface Condition

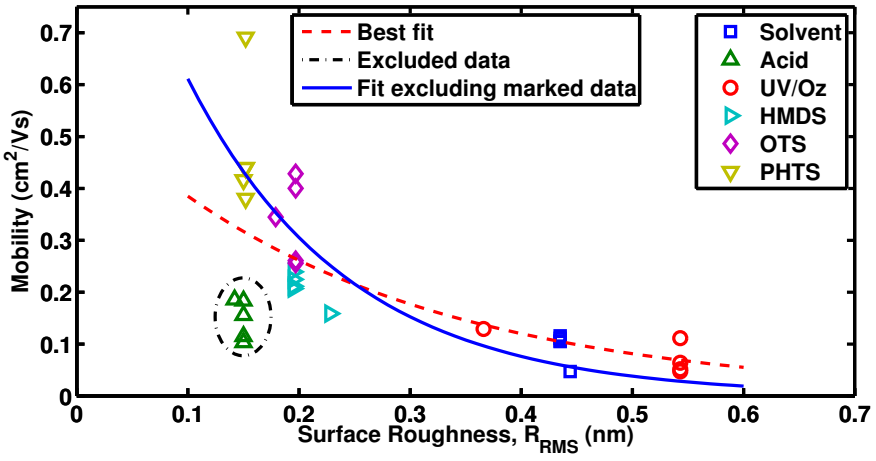
Referring to figure 4.28 it can be seen that there are various relationships between TFT device performance (field effect mobility, in this case) and material parameters such as pentacene grain size (4.28a), or dielectric surface properties such as roughness (figure 4.28b) and contact angle (figure 4.28c). In section 4.2.2.2 we examined the relationship between such surface properties and grain size. Now we must consider each of these and its relationship with electronic transport at the semiconductor-dielectric interface.

Firstly we consider grain size as a predictor of mobility. Figure 4.28a can at first sight appear to show little correlation between the pentacene grain size and device mobility. However, if only devices which have had either no surface treatment prior to pentacene deposition, or SAM treatment, are considered, then a strong positive correlation can be seen. It appears that for this subset of results, the widely accepted [93],[94],[95] and intuitive relationship holds true. An intrinsic intra-grain mobility, which is higher than that observed by terminal measurements, is approached as the number of trap-rich grain boundaries along a typical channel length reduces, due to the larger grains.

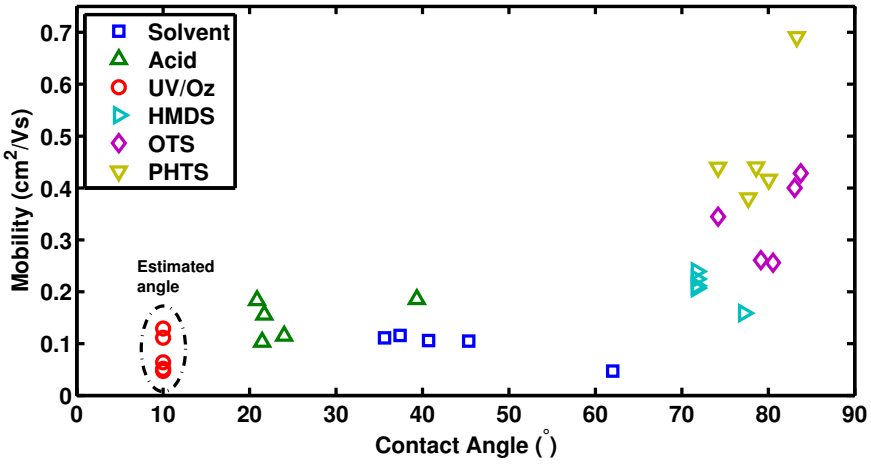
However, this analysis does nothing to explain the results seen with surfaces treated with acid or UV/ozone, where relatively large grains do not appear to



(a) Equivalent disk radius



(b) Dielectric surface roughness



(c) Water contact angle

Figure 4.28: Plotting the relationship between field effect mobility and various surface and grain characteristics for pentacene thin film transistors.

cause a significant enhancement in mobility over solvent cleaned devices.

Next we look at the relationship between surface roughness, which was earlier seen to have a strong relationship with grain size, and extracted mobility, as illustrated by figure 4.28b. In this case two fitted lines are plotted. Firstly (red-dashed) describing an exponential relationship between surface roughness and mobility according to the equation:

$$\mu_{fe} = \mu_0 \times e^{-\frac{R_{RMS}}{r}} \tag{4.2}$$

where μ_{fe} is the field effect mobility, R_{RMS} the root mean square surface roughness and μ_0 and r fitting parameters. Fitting parameter values for a fit of all data (dashed red line) are 0.57 cm^2/Vs and 0.26 nm respectively, while the equivalent values for the data excluding acid treated surface (solid blue line) are 1.22 cm^2/Vs and 0.14 nm. While the fit presented does not exactly describe the relationship seen, it can prove a useful guide and tool for beginning to understand device behaviour. The second fit provides a zero-roughness μ_0 value of 1.22 cm^2/Vs, which can be taken to the the trap free mobility which would be seen on a perfectly smooth surface. However, the very fact that a significant proportion of devices fail to agree with this model suggest that it may not in fact offer a useful estimate of future device performance.

Several possible origins have been suggested for the relationship between surface roughness and extracted mobility [96], with high grain boundary trap densities a likely cause of decreased performance [97].

According to the third presented relationship, shown in figure 4.28c, the water contact angle of each dielectric surface is plotted against mobility. While a strong correlation is not seen, a clear trend is visible, with no device category lying significantly outside the norm. It must be noted again that contact angle measurement for UV/ozone treated substrates were not taken, and the values plotted are estimated from the literature. However, that limitation aside, it appears that water contact angle, itself a strong indicator of (the inverse of) surface energy, provides the clearest indication of which surface will produce the highest mobility pentacene TFTs.

This can be understood with reference to similar results obtained by Shtein

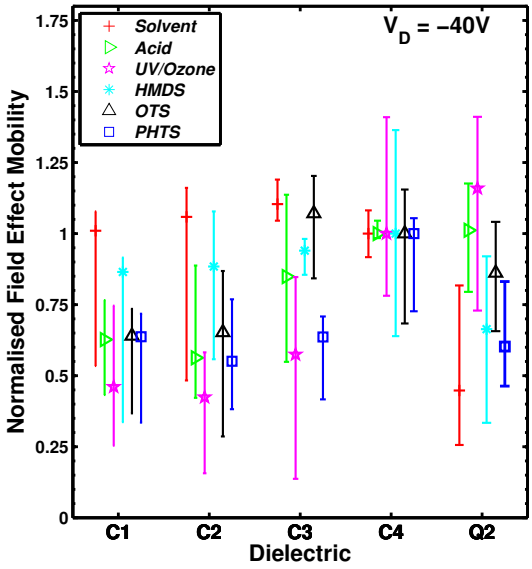


Figure 4.29: The relationship between field effect mobility and dielectric composition for pentacene thin film transistors. All mobility values are normalised to mobility of Si-rich SiN_x devices, 'C4'.

et al. [98]. In that work, it was suggested that the grain size itself does not control mobility directly, rather the effective adhesion of pentacene molecules to the dielectric interface.

4.3.2 Dielectric Composition

A further aspect of the substrate-performance interaction that must be considered is that of dielectric composition. In this work we have performed a number of surface treatments on a number of substrates with different gate dielectrics, allowing some comparison to be made between each. As can be seen from the normalised mobility values plotted in figure 4.29, for most surface treatments there is a trend of increasing mobility with increasing silicon content with the dielectric C1 ([N]/[Si] $\approx$ 1.7) typically having the lowest mobility, with C4 ([N]/[Si] $\approx$ 1.4) having the highest. Also shown in figure 4.29 are the normalised (to SiN_x C4) results for SiO_2, which are typically lower than those for Si-rich nitride.

Notably, this is not the case for solvent cleaned dielectric, where no such trend is apparent, with significant variation in mobility visible across a the number of

devices tested. Also anomalous is the enhanced mobility in OTS treated SiN_x films with a slightly lower silicon content, C3. However, the lowest silicon content films, C1 and C2 do follow this trend when treated with OTS.

In summary, devices treated with PHTS, OTS, HMDS, UV and acid all appear to perform best (highest mobility) when they are based on a Si-rich SiN_x, suggesting some advantageous property over the N-rich alternative. This result is in contrast with the choice of SiN_x typically favoured for use with amorphous silicon and nc-Si based TFTs [91, 99]. It can be seen from contact angle measurements that after the surface treatments considered in this study, the surface angle is similar for each dielectric surface. However, prior to patterning and surface treatment, extensive surface analysis was carried out on the pristine SiN_x surfaces, suggesting that in this state, there was more variation between surfaces. This analysis suggested that Si-rich surfaces were the smoothest of all considered (table 3.3).

A further effect to be considered is that the higher density of surface silicon atoms in Si-rich films can lead to improved SAM coverage. A higher number of Si surface atoms, when treated with oxidative surface treatments such as piranha cleaning and UV/ozone treatment will likely lead to an increased number of Si-O bonds at the surface, which are a necessary bonding site for the Si-terminated SAMs in use. This effect could explain the higher performance in SAM treated surfaces with high Si-content SiN_x films. As mentioned above, non-treated surfaces show little variation in mobility with different composition.

However, this does not explain the variation in performance of acid and UV/ozone treated surfaces with SiN_x composition. To much weight should not be placed on the UV/ozone based device results, as these show the most significant degree of variation between similar devices, suggesting that surface contaminants or irregularities are frequent.

In fact, considering again the morphological studies presented in figure 4.14 and in table 4.3, the HMDS treated surfaces show some of the largest variability in grain size of all surface treatments, suggesting a non-uniform coverage of HMDS.

4.3.3 Contact Resistance

As illustrated in figure 4.25, contact resistance values can be extracted for each family of devices from their electrical characteristics, also shown in table 4.4. While the contact resistance is here extracted independently of individual device parameters, owing to its dependence on several devices for extraction, it must be borne in mind when those parameters are considered. For example, the current observed in the 'on' state of all device characteristics will be suppressed by the injection barrier at each interface. These contact resistance estimates present a somewhat confused message at first sight, with a large degree of variation within each set of devices for a particular surface treatment, which should arguably have similar properties. The extraction mechanism used is susceptible to interference from variations in threshold voltage, and also non-linearities in threshold voltage itself. However, a number of general observations can be made:

- Solvent cleaned substrates tend to have the highest contact resistance
- UV/ozone cleaned substrates have a high degree of variation
- HMDS treated substrates have a high degree of variation
- Acid cleaned substrates often have the lowest contact resistance
- OTS/PHTS have widely varying results, but often are amongst the lowest contact resistances.

Considering the effect of each surface treatment on the contact-semiconductor interface can offer some potential explanations as to the mechanisms by which charge is transported across the interface. While conventional thinking would expect that a clean gold interface with the organic material should provide the most efficient charge injection, there is mounting evidence that suggests contact resistance can in fact be reduced by the presence of an ultra-thin barrier layer at the metal-organic interface. Li et al. have demonstrated a reduction in contact resistance of approximately 20 $\times$ by the UV/ozone treatment of Au electrodes in bottom contact small molecule organic TFTs [100], a similar result to that of Stablober et al. using pentacene [59]. A further report suggesting a similar effect

in top-contact OTFTs demonstrates the addition of a 1 nm barrier layer of various metal oxide materials, prior to contact deposition on top of pentacene thin films [101] where the contact resistance was reduced by an order of magnitude over the case where direct injection from Au was used.

An emerging view suggests that a direct metal organic interface is not optimal, even taking into consideration the expected work function of Au (≈5.1 eV) and the HOMO of pentacene (4.9 eV [102]), hole transport between the two has frequently been demonstrated to be limiting device behaviour. These results add weight to the argument that the interface may be improved the the presence of what may be of itself an insulating layer. In the case of the Au/pentacene interface, this interfacial layer will be in the form of a thin layer of AuO_x, formed by the application of either a piranha clean or UV/ozone treatment, or a combination of those processes.

4.3.4 Substrate Deposition Temperature

As discussed in chapter 3, a SiN_x process has been developed to produce high quality films at just 150 °C, with comparable performance to that previously seen in 300 °C films. We then briefly discussed devices fabricated on 300 °C SiN_x before turning our attention to 150 °C films. As has been shown in the latter part of this chapter, there appears to be no loss in device performance brought about by switching to the lower temperature dielectric. In fact, the highest device mobilities observed were on the presumed inferior dielectric. Other device parameters were comparable, suggesting that the 150 °C SiN_x produced was of a high quality and suitable for device applications. It must be borne in mind, however, that optimisation of the higher temperature film might yield improved results, however, adequate performance has been demonstrated in most respects.

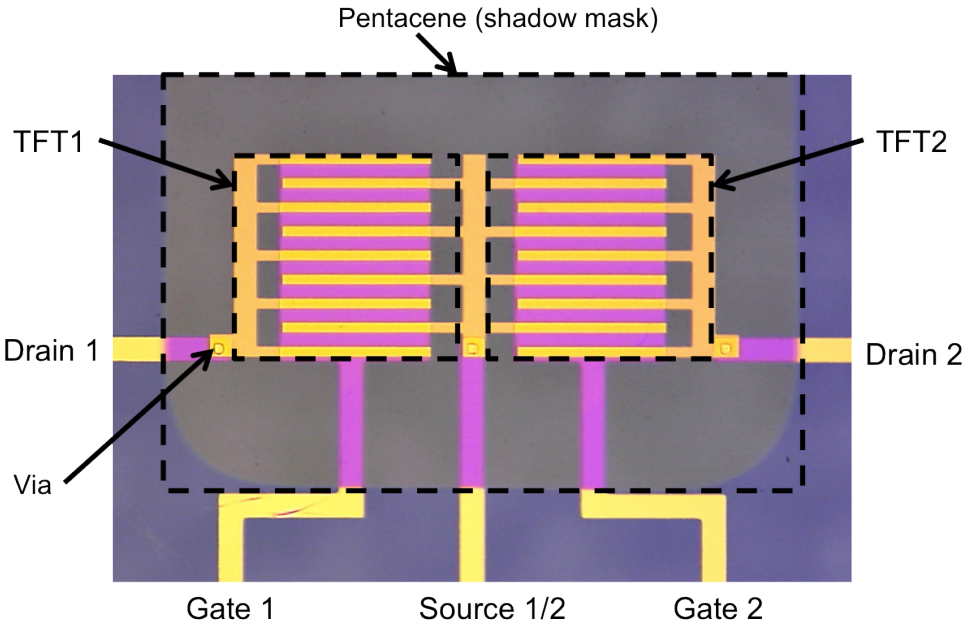
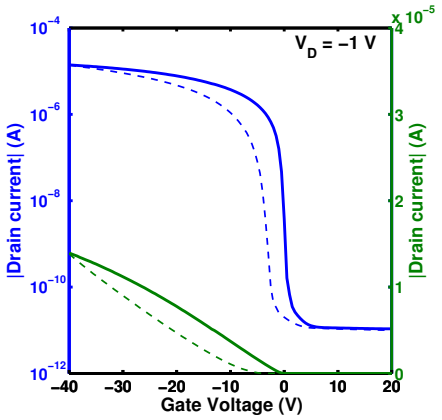


Figure 4.30: Micrograph of glass based TFTs showing channel regions.

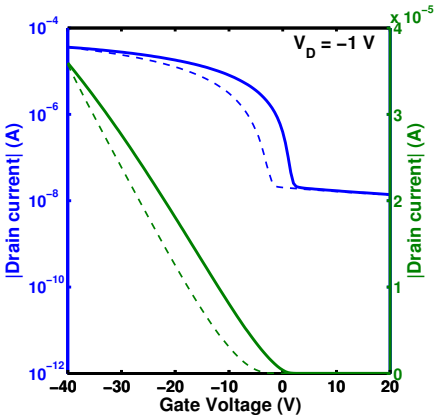
4.4 TFTs with 150 °C SiN_x Gate Dielectric on a Glass Substrate

While a successful demonstration of the use of a low temperature, plastic compatible, SiN_x dielectric is made with a popular organic semiconductor, thus far it has been demonstrated only with a common gate architecture. However, a series of devices have also been fabricated demonstrating the use of this dielectric on a glass substrate making use of a discrete gate architecture as shown in figure 2.1c. A micrograph of one such device is shown in figure 4.30. Electrical characteristics of glass-based devices with PHTS treated N-rich (a,c,e) and Si-rich (b,d,f) SiN_x dielectrics are shown in figure 4.31. Most striking from those figures is the extremely high 'off' current for devices based on a Si-rich dielectric. It is thought that this is likely to be due to the high conductivity of the pentacene material under no applied gate voltage, and is caused by a photolighography mask design problem.

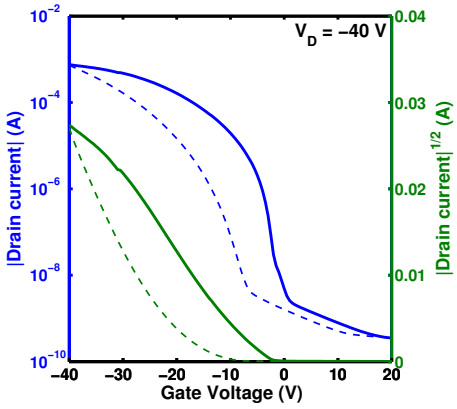
However, considering the TFT parameters extracted from these results, summarized in table 4.6, it appears that TFTs fabricated on a glass substrate do



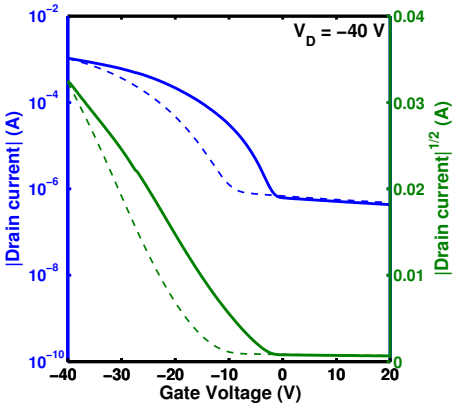
(a) Linear regime transfer: N-rich SiN_x



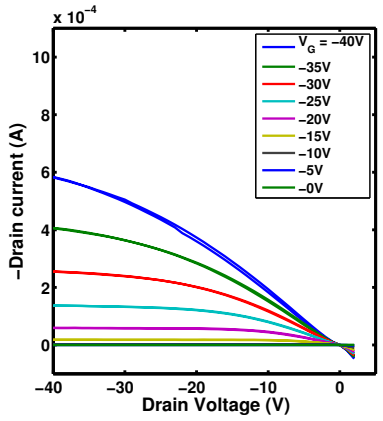
(b) Linear regime transfer: Si-rich SiN_x



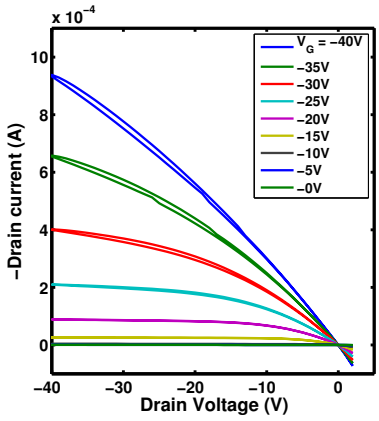
(c) Saturation regime transfer: N-rich SiN_x



(d) Saturation regime transfer: Si-rich SiN_x



(e) Output characteristic: N-rich SiN_x



(f) Output characteristic: Si-rich SiN_x

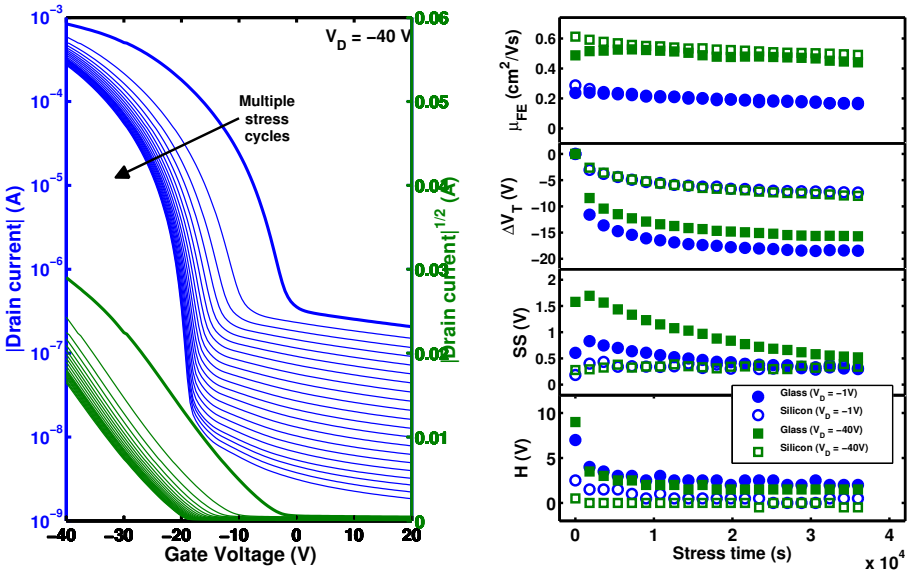
Figure 4.31: Electrical performance of pentacene TFTs on glass substrates with N and Si-rich SiN_x dielectrics.

Dielectric	Substrate	Mobility μ (cm^2/Vs)		Threshold Voltage V_T (V)		Sub-threshold Slope SS $(V/decade)$		Hysteresis H (V)	
	V_D (V)	-1	-40	-1	-40	-1	-40	-1	-40
C1	Glass	0.099	0.474	-1.2	-6.7	0.15	0.48	6.8	10.0
	Si	*0.073*	*0.440*	*-6.3*	*-9.7*	*0.19*	*0.28*	*5.8*	*2.2*
C2	Glass	0.147	0.510	-1.9	-6.9	0.16	0.63	6.5	10.0
	Si	*0.058*	*0.380*	*-7.3*	*-10.2*	*0.18*	*0.37*	*6.0*	*2.5*
C4	Glass	0.251	0.558	-1.2	-5.5	0.70	1.80	5.2	7.2
	Si	*0.363*	*0.691*	*-7.1*	*-6.8*	*0.28*	*0.32*	*2.5*	*1.2*

Table 4.6: Electrical characteristics of pentacene TFTs on PHTS treated SiN_x surfaces fabricated on glass (normal) and silicon (*italic*) substrates.

perform similarly to those previously considered on Si substrates. On average, mobility values are slightly reduced, while threshold voltage is also reduced. Sub-threshold slope appears high, for devices using Si-rich SiN_x an increase from $\approx$ 0.3 V/decade to 1.8 V/decade was observed. However, this significant increase is likely to be due to the true SS being masked by the high off-current. A further area of degradation in performance is in hysteresis, which increases from a few volts with Si substrate based devices to $\approx$10 V for glass based TFTs. It is thought that underlying surface roughness increases may be responsible for some of these performance issues, with parasitic and un-gated TFTs being responsible for the significant off-current observed.

To further understand the performance of glass-based devices, the Si-rich TFT was subjected to a similar bias-stressing procedure to that earlier used for several Si substrate based pentacene TFTs. The results of these measurements are presented in figure 4.32a, with a comparison made to Si-based devices in figure 4.32b. From these plots it can be seen that the initial high off-current reduces significantly over the stressing period, such that after 20 stress-cycles it has reduced by almost two orders of magnitude. This tends to support the idea that parasitic parallel TFTs are responsible for the current, as they too will be subject to a bias stress effect, by virtue of them conducting throughout the stressing period, albeit



(a) Saturation regime transfer curve **(b)** Parameter summary

Figure 4.32: Electrical performance of pentacene TFTs on glass substrates with Si-rich SiN_x dielectric under bias stress. Stress conditions: V_G = -20 V, V_D = -1 V, Stress period = 1800 s, Stress cycles = 20.

without an applied gate bias. As expected, as the large off-current subsides, the initially high sub-threshold slope gradually reduces to levels close to that seen in Si-based devices, suggesting that it was in fact just masked by a large off-current.

The comparison with Si-based devices (also Si-rich SiN_x shows clearly the close similarities in both linear (suppressed by high contact resistance) and saturation mobility. A more significant variation over stress-time is seen in threshold voltage, which shifts by more than twice as much as that seen in Si-based devices, by as much as 18.5 V. This large threshold voltage shift, taken with the large hysteresis observed in glass-based devices indicates a high density of charge traps at the semiconductor-dielectric interface. While surface preparation conditions were identical, it must be appreciated that rather than a perfectly clean and smooth substrate (Si) being the base for SiN_x deposition, glass based devices have a channel layer which is instead above gate metal (Cr deposited by thermal evaporation) and then PECVD SiN_x. It is thought that the introduction of a more closely controlled gate metallisation could yield a smoother surface onto

which to deposit subsequent layers.

4.5 Conclusions

In this chapter the effects of dielectric surface treatments on organic thin film transistors have been investigated, with common practices for SiO_2 based OTFTs being demonstrated to be successful on SiN_x based devices. High performance pentacene OTFTs were fabricated using a bottom-gate bottom-contact structure, initially on a 300 °C SiN_x, before being demonstrated with yet again improved performance on a plastic compatible 150 °C SiN_x, allowing a simple path to large scale device integration. A mobility enhancement of a factor of almost 8 was brought about by the use of a self-assembled monolayer (SAM) on high temperature (300 °C) SiN_x, while an improved baseline performance for a low temperature (150 °C) SiN_x results in a mobility enhancement of almost 5 by the introduction of a PHTS SAM on average over a number of substrate compositions.

Contact resistance in a series of devices was significantly reduced by the combination of the SAM treatment and an oxidative treatment to gold contacts, and while the degree of reduction varied between devices, it is clearly an avenue of device enhancement which can offer some benefit to those hoping to integrate devices using bottom contact geometries and conventional back-plane materials.

The composition of SiN_x dielectrics considered explored a range of [N]/[Si] ratios, and demonstrated that while an N-rich SiN_x is favourable for a-Si:H device fabrication, Si-rich SiN_x tends to perform better with small molecule organic semiconductors, with an average mobility enhancement of approximately 50% over the N-rich alternatives. An improvement of over 30% was seen over devices fabricated on an SiO_2 surface, suggesting that the relatively higher Si density at the surface can improve SAM adhesion and resultant surface condition. Si-rich SiN_x also proved to be the most stable of the SiN_x films.

The application of this high quality SiN_x film to glass based devices demonstrates the transferability of the process to alternative substrates, suggesting that the possibility of transfer to a plastic substrate should not be problematic.

These steps represent a novel combination of device structure and surface treatments, leading to OTFT fabrication strategy which is truly compatible with

existing large area electronic fabrication processes while also allowing the exploitation of new organic materials as they become available with minimum process modifications and limitations.

Limitations with the devices demonstrated are that they do not perform as well as devices with high quality (and high temperature) dielectrics in some respects, such as device stability. However, further work in this area is likely to allow the optimisation of surface treatment parameters which may go some way to overcoming such drawbacks.

Chapter 5

Copper Phthalocyanine Field Effect Transistors

Copper phthalocyanine (CuPc, figure 1.2b) is a small molecule organic semiconductor initially used as a synthetic dye, due to its strong blue colour. More recently it has become a popular photon absorber in organic photovoltaic (OPV) cells due to its optical absorption properties, absorbing strongly in the red (680nm) part of the spectrum. This fact coupled with the p-type semiconducting nature of the material allow it to be used in bulk heterojunctuon OPV devices. Thin film transistors based on CuPc have been reported for many years, with typical mobilities of 0.02 cm^2/Vs reported in film devices [38].

Hexadecafuorocopper phthalocyanine (F_{16}CuPc, figure 1.2c) is a CuPc derivative in which each of the 16 outermost hydrogen atoms are substituted for fluorine. The electronegativity of these F atoms significantly changes the electron density of the molecule, resulting in a predominantly n-type semiconductor, when used in conjunction with Au electrodes, in which the HOMO and LUMO levels are both shifted to higher energy states, as illustrated by figure 5.1. This results in a semiconducting material that while similar in many properties to CuPc, can provide a complimentary n-type TFT to the p-type TFT produced by CuPc, when used with an identical electrode material. Reported mobilites are up to an order of magnitude greater than those found in CuPc [103, 104].

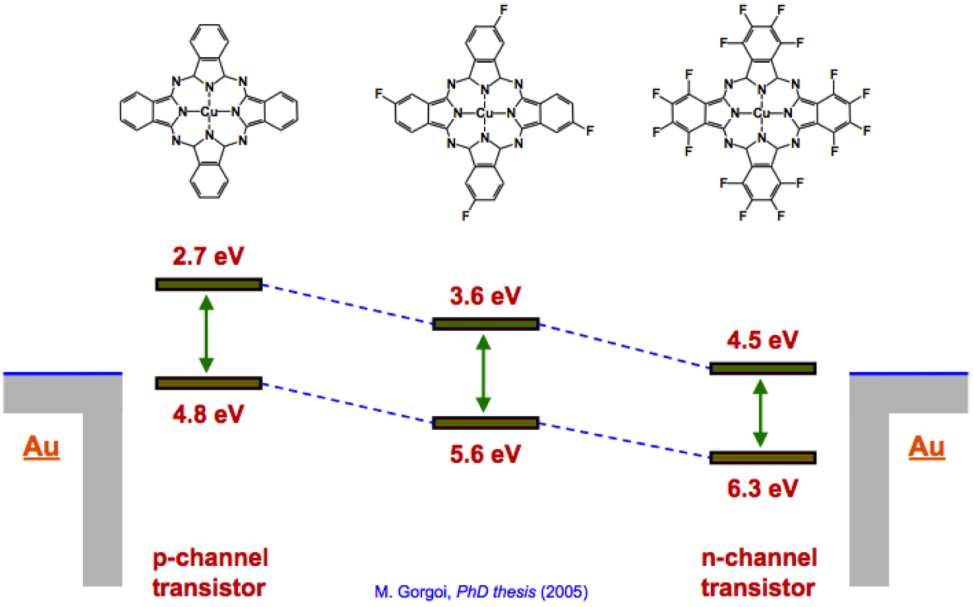


Figure 5.1: Schematic illustration of the HOMO and LUMO band alignment of CuPc, F_4CuPc and F_{16}CuPc, with reference to Au electrodes [3] (originally from [4]).

5.1 TFTs by Organic Molecular Beam Deposition

5.1.1 Device Fabrication

Crystalline silicon wafers coated with either SiO_2 or SiN_x as gate dielectrics, with lithographically defined Au/Ti contacts as described in Section 2.1, were used as a platform to investigate OTFTs using CuPc as the active semiconducting material. The CuPc source material was first purified in a tube furnace, before being collected and stored for use. Films were initially deposited by Organic Molecular Beam Deposition (OMBD).

All OMBD films were deposited using a Lesker Spectros system, shown schematically in figure 5.2, with four organic and three metal sources. This technique relies on passing an electrical current through a filament which surrounds a ceramic crucible, itself containing the source material. The heat generated by this current causes the material to sublime, and once a shutter is removed, a beam of organic

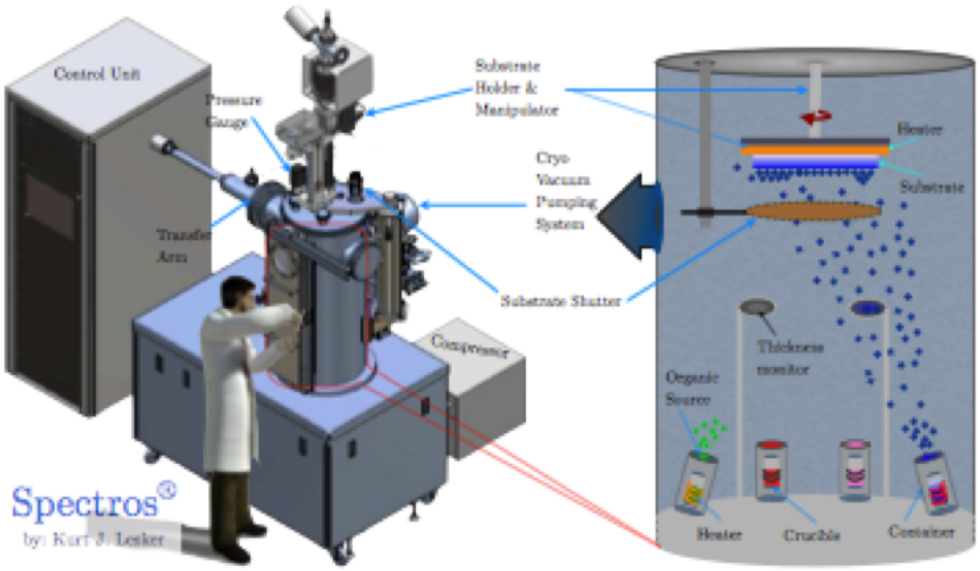


Figure 5.2: Schematic illustration of an OMBD system [5].

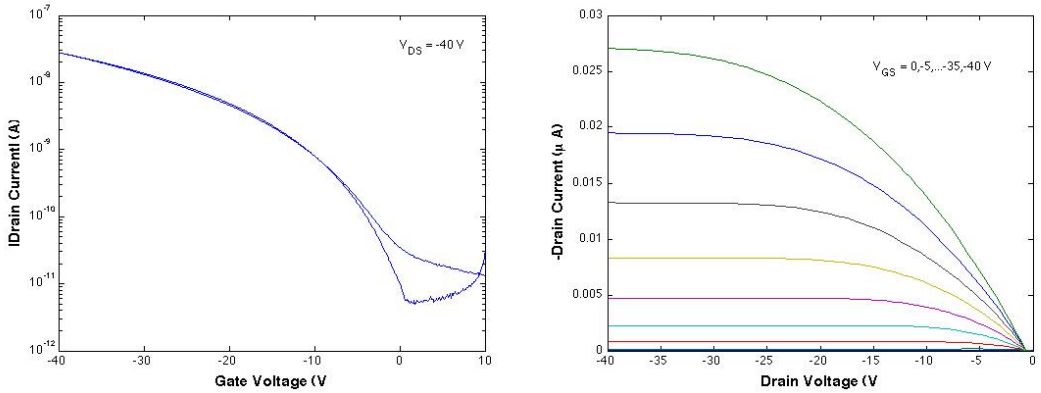
material is projected from the source describing a cone-shaped beam. Prepared substrates are loaded onto a sample holder, and placed in full view of this beam prior to deposition, at an approximate distance of one metre, and perpendicular to the beam. This large separation and the fact that the sample holder is rotated during deposition ensures that a uniform film is deposited. The system used also allows heating of the substrate during deposition by way of IR heaters. Films were deposited at a slow rate (0.1 $\AA$/s) to a thickness of 40 nm.

5.1.2 Device Characterisation and Parameter Extraction

5.1.2.1 Copper Phthalocyanine TFTs

Initial transistor characteristics were measured in the dark and under vacuum using an Agilent B1500A Semiconductor Characterisation System. Characteristic transfer and output curves are shown in figures 5.3a and 5.3b for a device with channel length of 50 μm and width of 500 μm on a SiO_2 dielectric.

The maximum extracted hole field effect mobility of this device is 3.4×10^{-3} cm^2/Vs, the threshold voltage -5.9 V, and hysteresis (at $I_{on}/10$) of just 0.3 V, all



(a) Transfer curve **(b)** Output curve

Figure 5.3: CuPc TFT chracteristics using SiO_2 dielectric. W = 500 μm, L = 50 μm

extracted from the saturation regime of operation at V_{DS} = -40V.

5.1.2.2 Fluorinated Copper Phthalocyanine TFTs

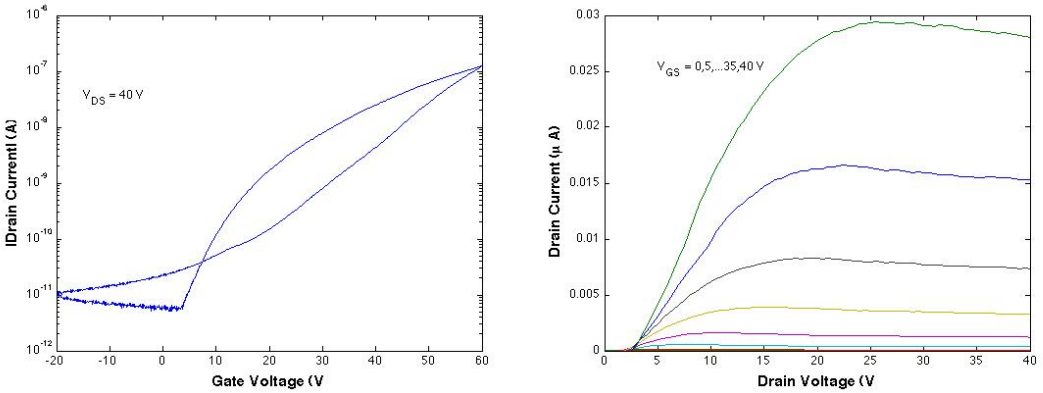
A similar process is used to deposit hexadeca-fluro-copper phthalocyanine (F_{16}CuPc), resulting in equivalent n-type devices to those previously demonstrated wit CuPc. Device characteristics can be seen in figures 5.4a and 5.4b, for a device similar to that already described based on CuPc.

The maximum extracted electron field effect mobility of this device is 1.5×10^{-3} cm^2/Vs, the threshold voltage 24.5 V, and hysteresis ($I_{on}/10$) 11.8 V, all extracted from the saturation regime of operation at V_{DS} = -40V.

These devices illustrate the baseline against which various other process conditions are compared.

5.1.2.3 Substrate composition

We further deposit films of CuPc and F_{16}CuPc on a number of different dielectric surfaces, and consider the effect of the substrate composition on TFT behaviour. Thermal SiO_2 and a number of SiN_x substrates, ranging from N-rich (C1, NH_3/SiH_4 = 20) to Si-rich (C4, NH_3/SiH_4 = 5), are used. The intermediate points are C2 (NH_3/SiH_4 = 15) and C3 (NH_3/SiH_4 = 10). The SiN_x materials



(a) Transfer curve **(b)** Output curve

Figure 5.4: F_{16}CuPc TFT chracteristics using SiO_2 dielectric. W = 500 μm, L = 50 μm.

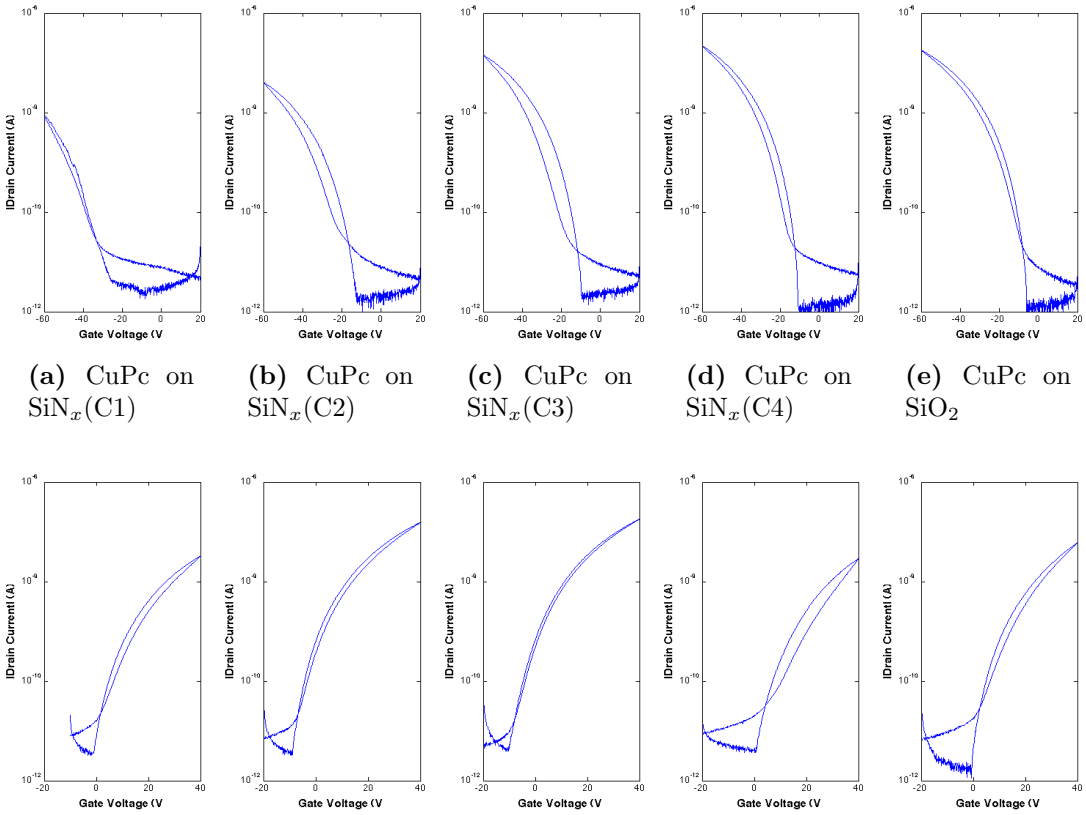
	Channel Length		SiO_2	SiN_x			
		SiH_4/NH_3	-	20	15	10	5
CuPc	10 μm	Mobility (x10^{-3} cm^2/Vs)	1.2	0.1	0.6	1.5	1.9
		Threshold Voltage (V)	-16.0	-20.9	-26.0	-23.7	-22.8
		Hysteresis (V)	5.0	4.7	7.5	6.8	4.0
	50 μm	Mobility (x10^{-3} cm^2/Vs)	1.5	0.5	0.5	1.5	2.3
		Threshold Voltage (V)	-20.3	-37.4	-25.8	-24.2	-24.4
		Hysteresis (V)	3.2	2.7	5.2	6.1	3.3
F_{16}CuPc	10 μm	Mobility (x10^{-3} cm^2/Vs)	1.3	0.2	1.8	2.2	0.5
		Threshold Voltage (V)	13.6	-0.3	-16.5	-17.4	11.8
		Hysteresis (V)	-2.8	-9.4	-2.0	-0.9	-5.5
	50 μm	Mobility (x10^{-3} cm^2/Vs)	1.3	0.5	1.7	2.0	0.6
		Threshold Voltage (V)	11.8	9.7	4.9	5.0	12.2
		Hysteresis (V)	-2.6	-2.9	-2.0	-1.1	-5.1

Table 5.1: TFT parameters for OMBD CuPc and F_{16}CuPc devices using SiO_2 and SiN_x dielectrics. W = 500 μm, L = 10,50 μm.

are discussed in more detail in chapter 3.

Figure 5.5 shows transfer curves in the saturation regime for each substrate and organic semiconductor combination, while table 5.1 and figure 5.6 summarise the extracted device parameters.

Significant observations:

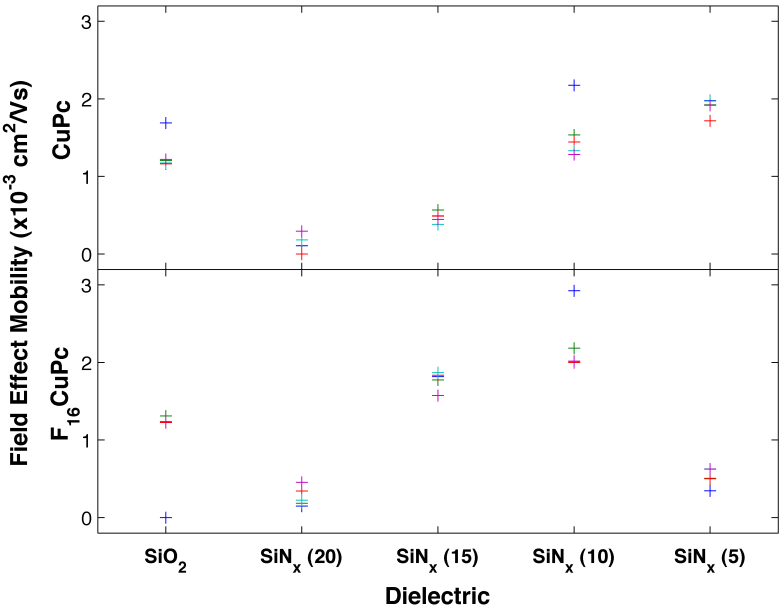


(a) CuPc on SiN_x(C1) **(b)** CuPc on SiN_x(C2) **(c)** CuPc on SiN_x(C3) **(d)** CuPc on SiN_x(C4) **(e)** CuPc on SiO_2

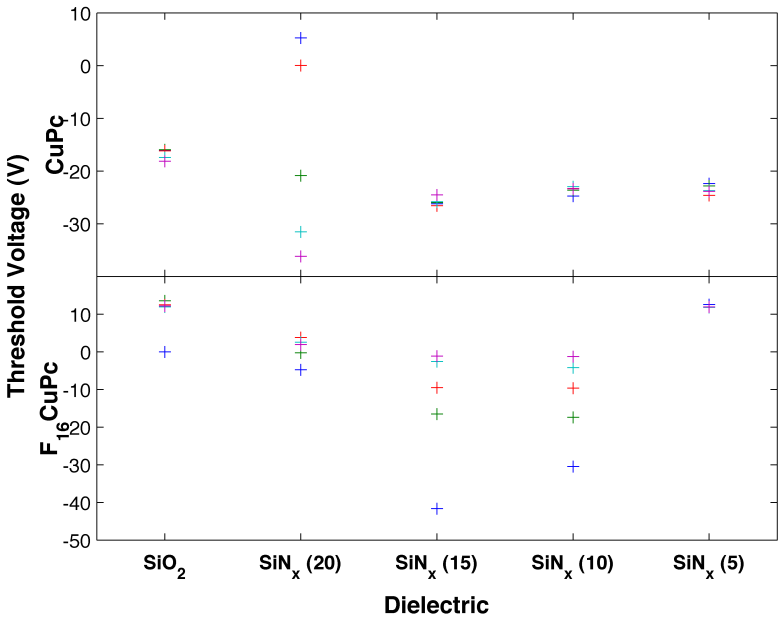
(f) F_{16}CuPc on SiN_x(C1) **(g)** F_{16}CuPc on SiN_x(C2) **(h)** F_{16}CuPc on SiN_x(C3) **(i)** F_{16}CuPc on SiN_x(C4) **(j)** F_{16}CuPc on SiO_2

Figure 5.5: CuPc and F_{16}CuPc TFT chracteristics using SiO_2 and SiN_x dielectrics. W = 500 μm, L = 50 μm.

- Mobility is highest with CuPc for SiN_x C3 and C4, which matches, and sometimes exceeds SiO_2 mobility.
- Mobility is highest with F_{16}CuPc for SiN_x C2 and C3, which matches, and sometimes exceeds SiO_2 mobility.
- CuPc on C1, and F_{16}CuPc on C2 and C3 show significant V_T variation as a function of channel length.
- V_T has shown shift towards 0 V with annealing treatment in the past.

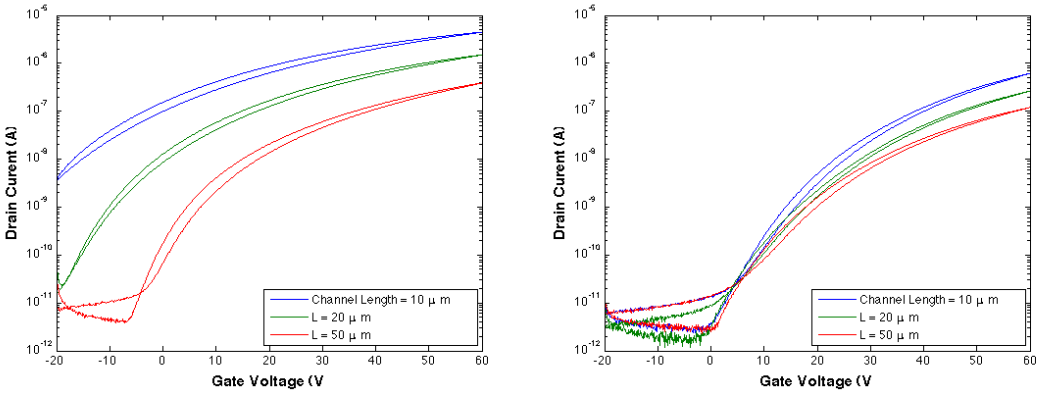


(a) Mobility variation



(b) Threshold voltage variation

Figure 5.6: Threshold voltage and mobility variation across various substrates with a selection of device lengths (5-50 μm). SiN_x (n) refers to NH_3/SiH_4 ratio during SiN_x deposition.



(a) Pristine condition **(b)** 45 minute anneal

Figure 5.7: Transfer curves for F_{16}CuPc TFTs on SiN_x before and after annealing.

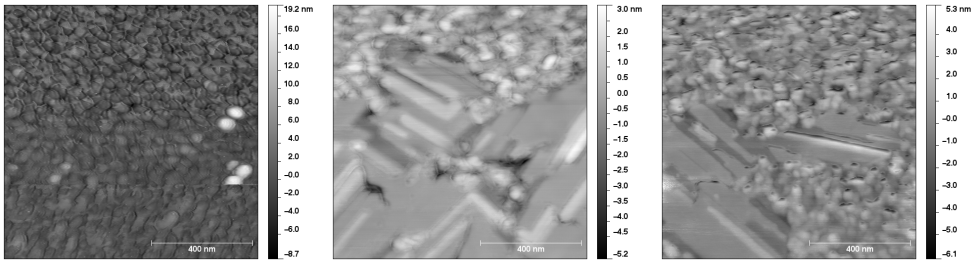
5.1.2.4 Annealing

Substrate C3 was selected for further study, owing to it producing the highest mobility devices. Only the large threshold voltage variation serves as a barrier to well performing devices.

Both CuPc and F_{16}CuPc films (25nm) were deposited on SiO_2 and SiN_x C3 substrates. Devices were subsequently annealed on a hotplate at 265 °C, under a dry nitrogen atmosphere, without yet having been exposed to oxygen. Some substrates were annealed at the same conditions prior to deposition.

The F_{16}CuPc samples on SiO_2 showed a significant enhancement in mobility after annealing, with a significant morphological change seen on inspection of the film by atomic force microscopy (AFM), figure 5.8. However, the same change was not observed for the SiN_x devices. The variation in V_T for these devices was reduced though, with devices of all lengths switching on at approximately the same voltage post-anneal, as can be seen in the transfer curves of relevant devices, plotted for channel lengths of 10, 20 and 50 μm in figure 5.7.

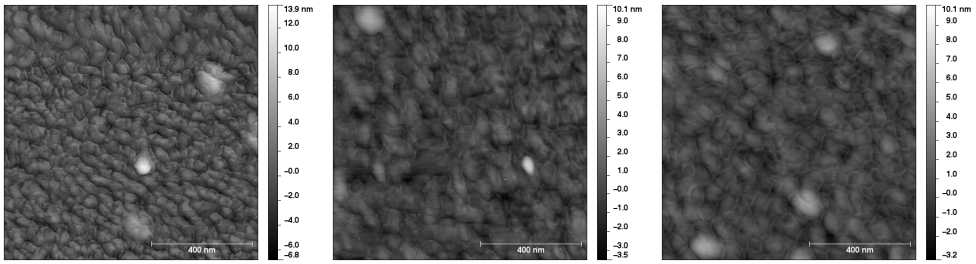
To further investigate this phenomenon a similar process was repeated, using a pre-deposition anneal of the substrate (at 265 °C) and a lower temperature, post-deposition anneal, so that any morphological change could be ruled out. While the mobility enhancement of the earlier process is not repeated, the V_T correction still occurs in the SiN_x, suggesting two processes occur, one activated



(a) SiO_2:pristine condition

(b) SiO_2:45 minute anneal

(c) SiO_2:90 minute anneal



(d) SiN_x:pristine condition

(e) SiN_x:45 minute anneal

(f) SiN_x:90 minute anneal

Figure 5.8: AFM images of $F_{16}CuPc$ on SiO_2 and SiN_x after various annealing treatments.

by a lower temperature than the previous 265 °C anneal.

It was also seen that annealing substrates before the deposition also brings about a significant mobility enhancement, and also corrects the V_T variation in SiN_x. This process may well be due to surface dehydration. Although all substrates are cleaned prior to deposition, a short O_2 plasma to remove photoresist residues may well be too short to fully dehydrate the surface. A (relatively) high temperature anneal may complete this process.

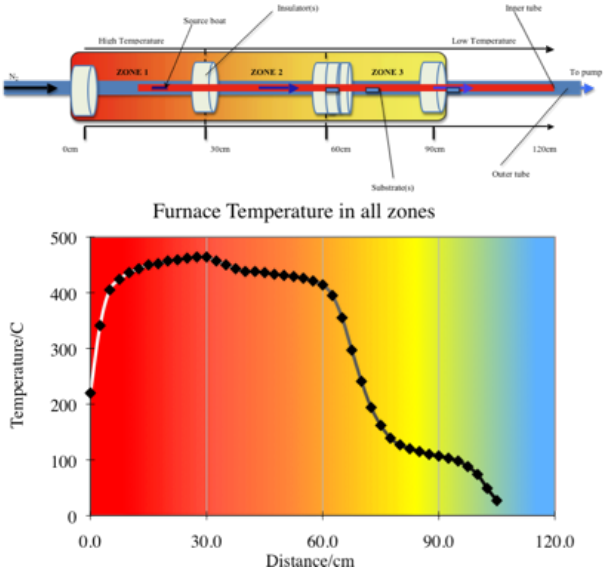
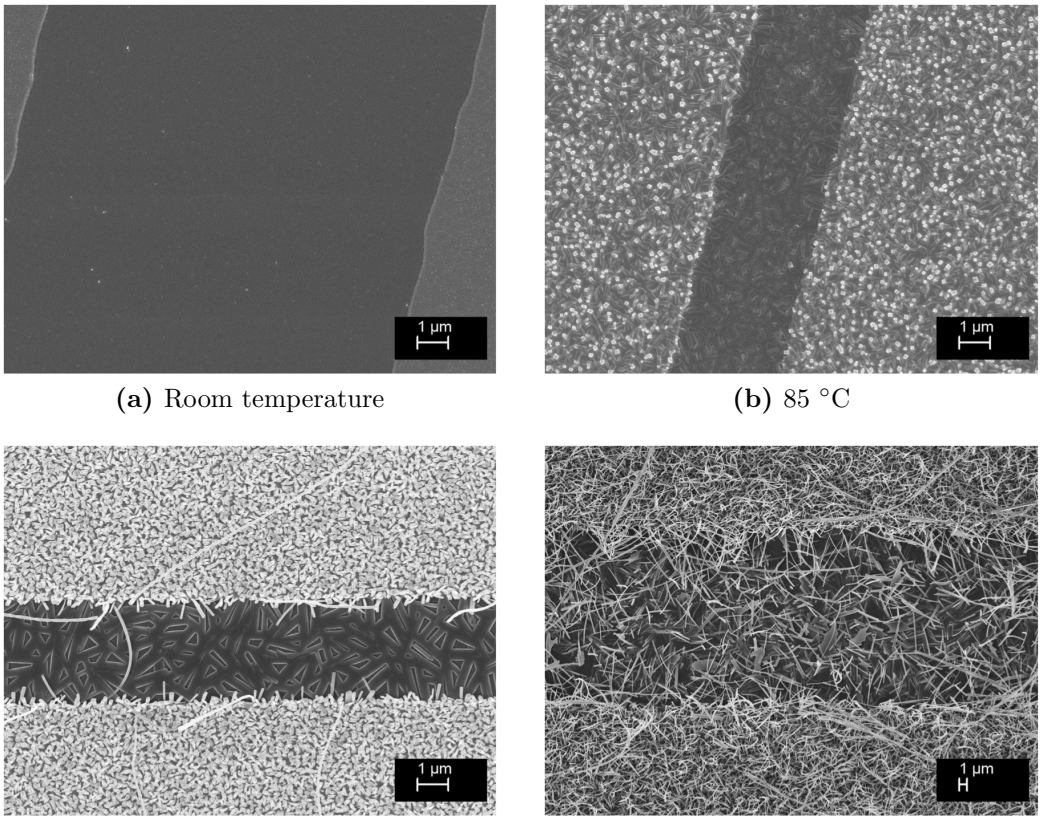


Figure 5.9: Schematic illustration and temperature profile of an OVPD system [5].

5.2 TFTs by Organic Vapour Phase Deposition

While until now we have considered only devices deposited under high vacuum by OMBD, Organic Vapour Phase Deposition (OVPD) offers an alternative to forming thin films on a pre-patterned substrate. OVPD makes use of a high temperature tube furnace, within which a crucible of source material is placed, and through which an inert carrier gas is passed. A typical OVPD system is illustrated in figure 5.9. As the source material is heated beyond its sublimation point it sublimes, and is carried along the tube by the carrier gas. As it reaches a cooler region of the tube it begins to condense on whatever surfaces are present.

Depending on the temperature gradient, gas flow rate, pressure and substrate organisation, it is possible to achieve a large number of different film morphologies and nanostructures from any given source material. As such, we investigate a number of different process conditions, with a view to fabricating high performance thin film transistors, and nanowire transistors.



(a) Room temperature **(b)** 85 °C

(c) 200 °C **(d)** 350 °C

Figure 5.10: SEM images of OVPD CuPc at various substrate temperatures using a SiO_2 dielectric. [Images by S.Din]

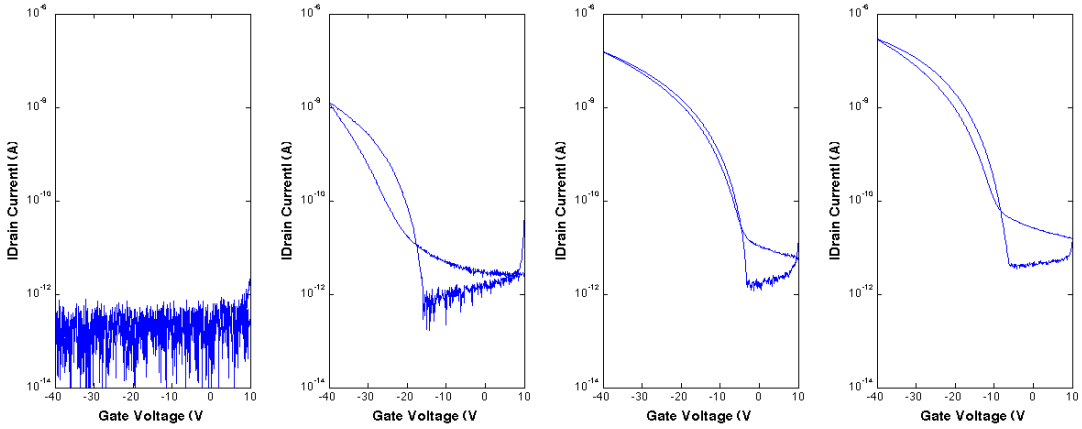
5.2.1 Device Fabrication

Both SiO_2 and SiN_x substrates were placed at pre-determined locations along a tube furnace, with temperatures known to be 350 °C, 200 °C, 85 °C and room temperature (approximately 21 °C), with nitrogen gas flowing through the tube at 350 sccm, and a base pressure of 6 mbar. After a controlled duration substrates were removed from the furnace, and immediately transferred to a vacuum probe station, where transistor characteristics were measured.

5.2.2 Device Characterisation and Parameter Extraction

Figure 5.10 presents SEM images of CuPc films in each of the different temperature regions. What is immediately apparent is that at higher temperatures a complex network of nanostructured CuPc is formed on the device surface. As the temperature is reduced, a less chaotic arrangement is visible, with the film seen at 85 °C closely resembling the morphologies observed in OMBD devices, while at room temperature an extremely thin film is formed.

Figure 5.11 shows transfer characteristics for devices formed on SiO_2 at the various temperatures, using a drain-source voltage (V_{DS}) of -40V, each device having a channel length of 50 μm and a width of 500 μm.



(a) Room temperature **(b)** 85 °C **(c)** 200 °C **(d)** 350 °C

Figure 5.11: Transfer chracteristics of OVPD CuPc TFTs at various substrate temperatures using a SiO_2 dielectric. W = 500 μm, L = 50 μm

From these plots a clear trend is visible, with higher on-currents seen in the higher temperature devices. The 'room temperature' device shows no current. The film deposited here is not thick enough to provide a continuous path for conduction. From the characteristics shown, TFT parameters were extracted, and are summarised in table 5.2, along with results from devices of different lengths and those fabricated using a SiN_x gate dielectric.

Channel Length	Temperature (°C)	SiO_2 85	SiO_2 200	SiO_2 350	SiN_x 85	SiN_x 200	SiN_x 350
10 μm	Mobility (x10^{-3} cm^2/Vs)	0.6	5.3	7.6	0.9	1.7	6.0
	Threshold Voltage (V)	-15.3	-9.9	-11.7	-16.7	-14.4	-14.5
	Hysteresis (V)	10.5	2.6	3.5	9.5	5.4	4.0
20 μm	Mobility (x10^{-3} cm^2/Vs)	0.7	4.1	6.5	-	1.4	5.9
	Threshold Voltage (V)	-20.2	-11.9	-16.0	-	-19.6	-17.5
	Hysteresis (V)	6.5	1.5	2.4	-	2.7	3.2
25 μm	Mobility (x10^{-3} cm^2/Vs)	0.5	3.8	5.8	-	1.3	5.9
	Threshold Voltage (V)	-20.2	-11.8	-14.5	-	-19.5	-16.9
	Hysteresis (V)	6.3	1.5	2.6	-	2.6	3.4
50 μm	Mobility (x10^{-3} cm^2/Vs)	0.7	3.0	5.5	1.9	0.9	6.2
	Threshold Voltage (V)	-19.7	-11.7	-13.2	-21.5	-20.1	-17.9
	Hysteresis (V)	5.1	1.3	2.9	5.1	2.1	3.3

Table 5.2: TFT parameters for OVPD CuPc on SiO_2 and SiN_x dielectrics

5.3 Copper Phthalocyanine Nanowire Field Effect Transistors

Semiconductor nanowire (NW) devices have become an exciting class of device in recent years. A number of materials' systems have contributed to the sense that recent developments in bottom-up self-assembly at the nanoscale can bring about any number of previously unattainable results [105], with applications in electronics [106], photonics [107, 108], biochemical [109] and chemical sensors [110].

More specifically, organic nanowire transistors offer a device structure that can allow the exploration of transport mechanisms within small-molecule and polymer materials previously only used in thin film devices. The fabrication of one-dimensional, single-crystalline organic nanowires, making use of self-assembly, promises to unlock device performances to rival those seen in well established large area back-plane technologies such as amorphous silicon [111].

As reported elsewhere [6, 5], several stable morphologies of CuPc exist. One of these, recently classified as the η-phase, can take the form of wires approximately 100 nm in diameter and several 100s of μm in length. SEM and optical images of such wires are shown in figure 5.12. Clearly there are a large number of interconnected wires, forming a seemingly random network. The challenge in device fabrication is to make electrical connections to these wires to allow electronic transport along the length of the wire, making use of the anticipated enhancement in mobility brought about by the reduction in grain boundaries over the film alternatives previously studied.

Several examples of CuPc nanowire devices exist, such as those demonstrated by Tang et al. [112]. Ribbons of β-CuPc are synthesised by physical vapour transport with observed dimensions being in the range of hundreds of nanometres wide and 5-10 micrometers in length. Individual ribbons were isolated and transferred to an experimental dielectric coated substrate using a microprobe, with metallic source and drain contacts formed by thermal evaporation, using a wire as a mask to create a channel region. The channel length of the device used in this case was approximately 10 μm, and the width 200 nm (the width of the CuPc ribbon in question). Field effect mobilities extracted were 0.1-0.2 cm^2/Vs,

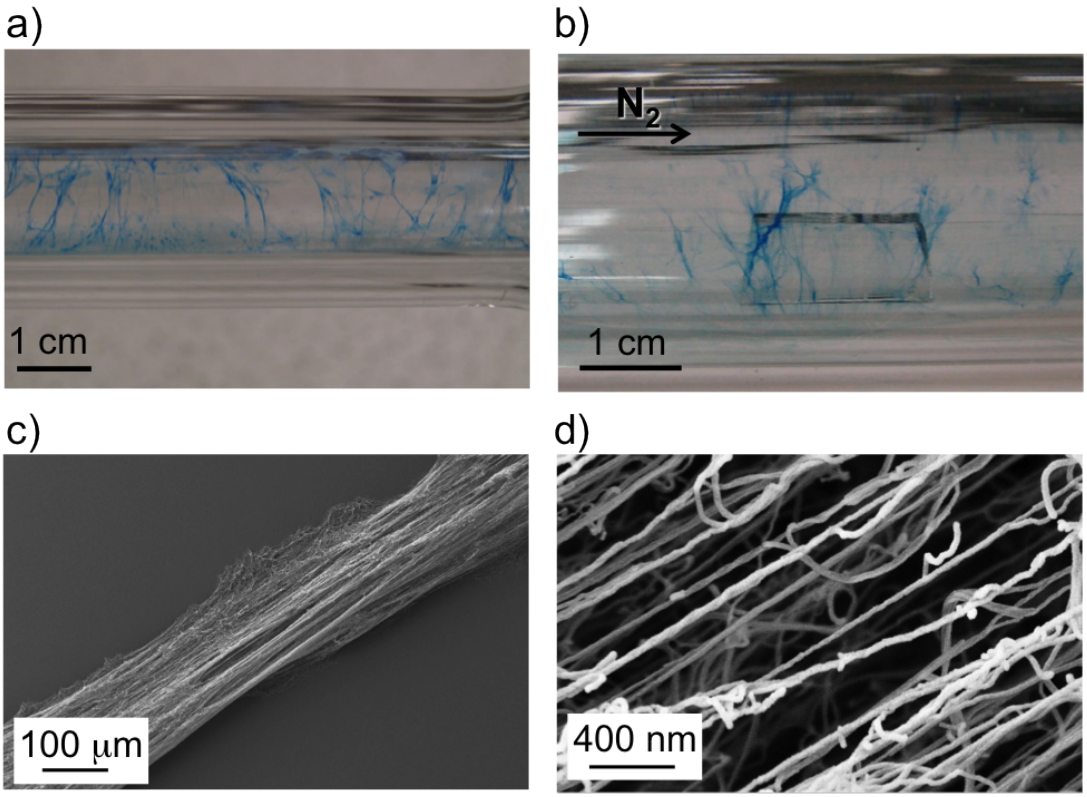


Figure 5.12: Photographic and SEM images of η-CuPc branches and nanowires. Digital photographs showing the growth of CuPc branches inside the quartz tube (a) and on a glass substrate (b). SEM image of a single η-CuPc branch showing bundles of nanowires (c-d) [6].

a high value for CuPc devices.

Tang et al. have also gone further than individual devices, integrating both wires of p- and n-type CuPc derivatives (p-type: CuPc, n-type: F_{16}CuPc) to fabricate CMOS integrated circuits [113]. With similar devices and techniques to those reported above [112], these devices show a relatively high carrier mobility of up to 0.65 cm^2/Vs for electrons, or 0.1-0.61 cm^2/Vs for holes, a significant enhancement over the previous work of the group. These carrier mobilities are far in excess of those seen in film devices, which are typically of the order of $10^{-2}cm^2/Vs$[38].

The mechanical flexibility has also been studied by the same group [114], with results proving that flexible applications are a real possibility with this class

of material. An apparent enhancement in device performance of wires under strain also raises the possibility of their use as sensors, while suggesting that the interplane stacking dimension, when reduced, can lead to enhanced carrier mobilities.

A CuPc nanowire photoswitch was recently demonstrated by Cheng et al. in [44], showing current modulation of 100% under modest illumination. Here a hole mobility of 0.02 cm^2/Vs is quoted. 4 tetra(2-isopropyl-5-methlphenoxy) copper phthalocyanine nanowires were synthesised chemically by self-assembly. Wires were dispersed in ethanol, before being spin-coated on a substrate with predefined contacts, much like those used in this study. However, the poor device output characteristics exhibited here, with a significant ohmic contribution, suggest some kind of contaminant, possibly from the fabrication procedure. While a single wire has been isolated and identified bridging adjacent contacts, it is possible that other wires, or fragments thereof, are bridging at other positions with unknowable contributions to the terminal characteristics.

Another implementation of vapour-phase synthesised CuPc NW transistors has been demonstrated out by Xiao et al. [43]. In this case the nanowires are determined to be α-CuPc, and exhibit hole mobility of 0.4 cm^2/Vs. The wires were again controlled by micromanipulation, employing an organic ribbon masking technique [115] yielding individual wire devices.

In the related field of polymer materials, it is possible to create nanowire arrays by contact printing [116], yielding an array of well aligned nanowires which can use applied to thin film transistors. However, this approach is not available for use with non-soluble small-molecule organic materials such as CuPc.

As shown, a number of potential strategies exist for the fabrication of organic nanowire field effect transistors, ranging from bottom-up self-assembly techniques, to top-down lithography. Having considered some important prior art, we further discuss the applicability of each process to our NWs, objectives and present capabilities. This work then seeks to explore alternative device geometries and fabrication techniques to allow further exploitation of these newly described material morphologies. Several approaches are attempted, with results discussed.

5.3.1 Nanowire Growth

This work is carried out in close collaboration with Salahud Din, whose PhD thesis [5] contains extensive details of the nanowire growth mechanisms and techniques employed. Organic vapour phase deposition (OVPD) is well known to generate a number of varied film morphologies when used with small molecule materials such as CuPc. Smooth films, textured surfaces and nanowires have all been demonstrated to be possible in a dual tube furnace, with the morphology under control of the local conditions within the tube. Optimised growth conditions yield repeatable depositions of several morphologies, with targeted substrate placement enabling a particular morphology to be collected.

5.3.2 Device Preparation

While the wires discussed are grown using similar conditions to the OVPD films previously described, the nature of the wires requires a significantly different approach to transistor fabrication. Several different NW FET fabrication strategies have been identified and explored.

A most basic approach is to grow NWs directly onto a pre-patterned substrate, much has been described for CuPc TFTs previously. However, it is likely that wires do not form a continuous and uniform 'film' between contacts, leaving conductivity highly variable in nature when compared from one device to the next. To explore this assumption, pre-defined substrates were placed along a furnace in positions known to produce different densities of NWs, and the resulting 'films' investigated. While direct control of position and wire morphology cannot be guaranteed, by studying several similar depositions, and closely controlling growth parameters it is possible to predict, with a high degree of accuracy the form of the deposition on a particular substrate.

Building on this technique is a method developed to deposit wires preferentially on one area of a substrate, with two possibilities considered. Firstly, a simple shadow mask can be applied to the growth substrate, meaning material is only deposited in the exposed regions. An extension to this method is then tried. By extending the mask in the vertical plane, the carrier gas can be channelled to a targeted region, resulting in a higher flow and hence increased local density of

organic molecules leading to higher deposition rate.

While in situ growth allows the simplest of fabrication procedures, it has also been demonstrated that growth on a temporary substrate can be used, followed by the transfer of wires to a substrate more suitable for use in electrical devices. For example, where processing conditions are harsher than a substrate can be exposed to, a more hard-wearing material can be used as a growth substrate. Another example could be where a nucleation layer or catalyst is employed for nanowire growth, which would not be suitable for use in electrical devices. This technique has the disadvantage that some mechanical action may cause damage to the wires, but allows regions of high wire density to be targeted and effectively harvested. It may be necessary in this process to use a solvent to assist in transfer, which will subsequently evaporate leaving behind NWs on any surface. Both techniques have been explored, with preference for the non-solvent assisted technique due to the potential for introducing contaminants, or partial dissolution of the NWs leading to damage.

A number of examples exist of such a practice in the literature, such as its application to the transfer of carbon nanotubes for use in TFTs [117] or with In_2O_3 nanowire mats by Shen et al.[118]. Any number of demonstrations have been made of wires being dispersed in solution to allow a low density (single wire) device to be fabricated.

Finally, attempts were made to identify and connect individual NWs using the combination of SEM (imgaging) and FIB (contact deposition). With this technique it is possible to define structures of similar dimensions to the NWs studied, and position them with even greater accuracy. However, FIB is resource and time intensive way of forming nanostructres, which also introduces significant radiation to the system. The effect of both electron, and ion radiation damage must be assessed.

A detailed discussion of each of these techniques follows.

5.3.2.1 In Situ Growth

This technique simply requires the placement of a pre-patterned TFT substrate in the nanowire growth assembly. By careful selection of growth position, it is

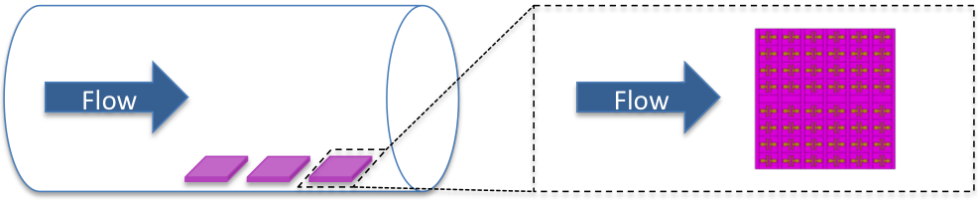


Figure 5.13: Schematic illustration of a tube furnace, with substrates placed in the tube, onto which wires are deposited.

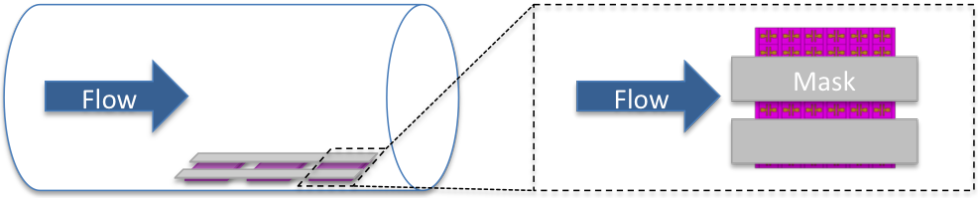


Figure 5.14: Schematic illustration of a tube furnace, with masked substrates placed in the tube, onto which wires are deposited.

possible to achieve a high degree of control over the morphology and density of NWs deposited on the growth substrate. However, wire alignment and nucleation points appear to be entirely random. As such, a large number of wires can be deposited on a transistor channel area, however wires will also be deposited in undesirable regions, potentially creating complex interactions between devices, and possible short-circuits.

5.3.2.2 Masked growth

By masking some regions of the growth substrate it was expected that it might have been possible to grow wires in a chosen region, patterned by the careful placement of the mask, as illustrated in figure 5.14. However, on initial trials it became clear that wire adhesion to masking material was similar to that of the substrates, and in fact wire penetration of the mask was poor, leading to a significant majority of wires being removed with the removal of the mask.

While individual wires are extremely small, they tend to clump together, possibly by virtue of some form of static attraction, meaning that rather than a fine and uniform distribution of wires there tends to be found a number of bundles of wires. It is also true that when an obstruction is placed in the path of the

carrier gas during OVPD growth wires tend to cluster on the leading and trailing edges. This would suggest that in regions of turbulence, where the laminar flow is disturbed by some abrupt edge, there is a higher nucleation rate of NWs. Once nucleated, the relatively larger number of wires in this region grow by effectively collecting more material from the carrier gas as it passes by, exaggerating the non-uniform distribution of wires still further.

By manipulating the carrier gas flow it is possible to 'focus' the areas in which the wire density is at its greatest, enabling effective targeting of deposition material on carefully placed substrates. This procedure was found to be reliable at producing similar wire depositions.

5.3.2.3 Post growth transfer

As shown by Shen et al. [118], useful devices can be created by transferring material post-growth to a more useful substrate. In our work, we were able to collect deposited nanowires from the internal surface of a tube furnace, either directly, or by using a kapton film to line the internal surface, and subsequently transferring wires to a pre-prepared substrate. Figure 5.15 illustrates the technique used. A mat of wires is removed carefully from the tube furnace, before being transferred to a substrate by dragging the substrate over the surface of the mat, leaving wires attached to the surface of the substrate. As has been shown in several studies [6, 114], CuPc nanowires are mechanically strong, with a good ability to recover from deformation. While some damage is likely through wires being crushed, it is hoped that a large proportion of wires will be transferred with no damage.

5.3.2.4 Focussed Ion Beam

Focussed ion beam (FIB) is a technique which simultaneously uses a scanning electron microscope (SEM) to image a sample, while a second beam, of Ga ions, is used in conjunction with an organic gas to deposit material. A gas precursor is introduced into the sample space local to the intended deposition site, while the incident ion beam serves to crack the adsorbed gas molecules, leaving a residue of metal behind. Using this technique it is possible build extremely fine featured wires, with resolution as good as 10 nm readily achievable. As a technique it

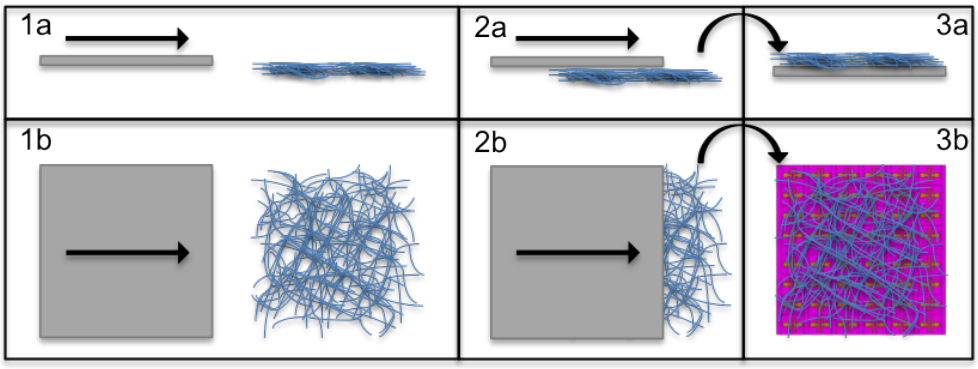


Figure 5.15: An illustration of a post-growth nanowire transfer technique. In step 1 (1a plan view, 1b side view) a mat of NWs is shown with an inverted substrate. At step 2 the substrate is dragged over the wire mat. At step 3 substrate is once more inverted, with wires attached.

has been used many times to make contact with nanostructured items, such as zinc oxide tetrapods. We have attempted a similar process with CuPc nanowires grown by OVPD.

It is important to note, however, that reports exist of damage being done to OFET devices after irradiation with electron-beams [112].

Results presented here represent devices fabricated by in situ growth, in which the carrier gas flow had been channelled to focus deposition on locations in which pre-patterned substrates were positioned. This process represents a reliable method for achieving relatively high density and uniform distribution of wires on each substrate, with a high degree of probability that any device will perform well after fabrication.

5.3.3 Device Characterisation

5.3.3.1 Microstructure

To gain an accurate understanding of the electrical properties of the NW FETs produced it is essential to characterise the structure of the conducting path from one electrode to another. Several potential arrangements of wires are illustrated in figure 5.16(a-c). Each of these may occur on consecutive devices on any substrate, and as such, efforts must be made to relate electrical behaviour to channel con-

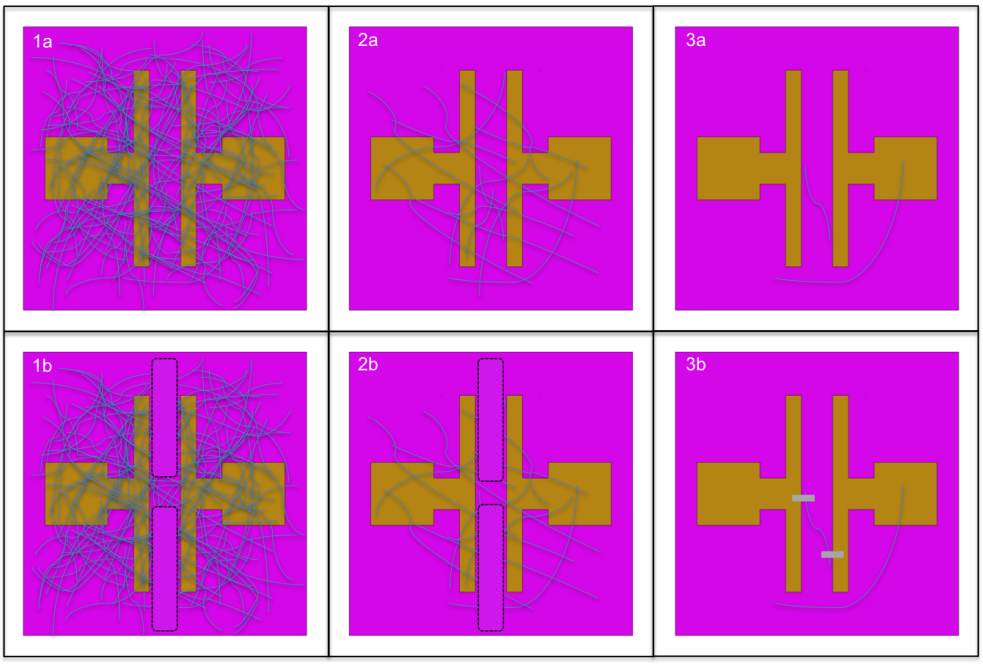


Figure 5.16: Various approaches to using a Focussed Ion Beam to create well defined NW transistors: 1) dense wires (1a) can be removed to leave a small active region (1b), 2) sparse wires (2a) can be removed to leave a single wire bridging source and drain contacts (2b), and 3) isolated wires (3a) can be contacted by FIB deposited metallic contacts (3b) to bridge source and drain contacts.

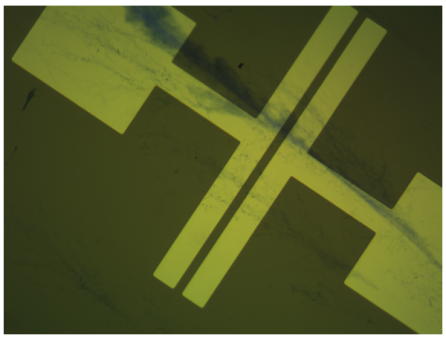
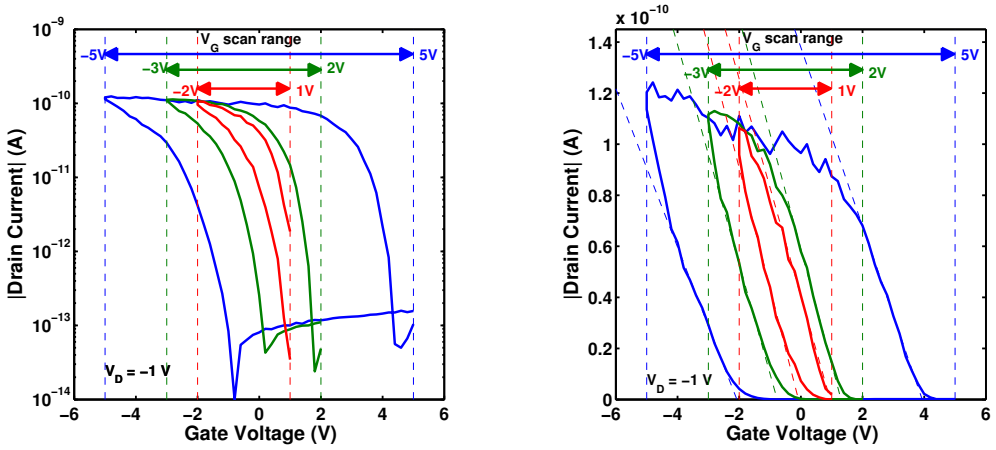


Figure 5.17: Optical micrograph of CuPc nanowires on TFT substrate (image:S.Din)



(a) Logarithmic scale **(b)** Linear scale

Figure 5.18: Transfer characteristics of a CuPc nanowire field effect transistor with different gate voltage scan ranges (-5V:+5V, -3V:+2V and -2V:+1V). Channel width 500μm, length 5μm.

figuration. If it is hoped to perform electrical measurement after characterisation then the technique employed must be non-destructive, such as AFM. Alternatively, it may be possible to perform electrical characterisation, and subsequently examine devices with techniques such as SEM, which will allow a larger area to be imaged easily, although will likely damage the FETs in the process due to the charging of delicate regions of the device as a result of electron bombardment. A typical NW device is shown in figure 5.17.

5.3.3.2 Electrical Characterisation

The electrical behaviour of NW FETs is highly dependent on many factors involved in their fabrication and measurement. We seek to understand the underlying behaviour of the materials involved by examining a large number of devices.

Electrical characterisation of NW FETs was carried out both in vacuum, and under atmospheric conditions, with similar results achieved in both instances, initially. However, once devices are exposed to air for a significant duration of time changes in device behaviour have been observed, whereby the devices begin to exhibit a significant hysteresis in turn-on and turn-off behaviour. Such behaviour

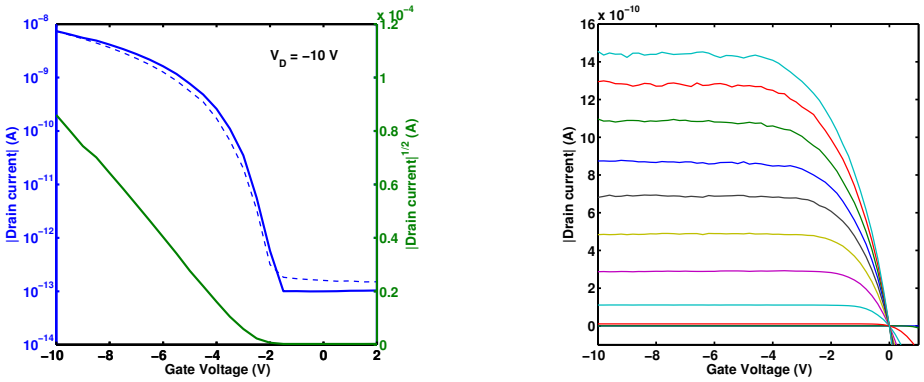
has previously been observed in TFTs also fabricated from CuPc, but not to the extent observed here in NW devices. In some cases many volts difference in turn-on and turn-off are observed, with the almost any value achievable with different driving schemes, as illustrated in figure 5.18.

In this example, driving the device with an initial gate voltage of +5V resulted in a turn-on threshold voltage of +4V. Having then swept the gate voltage to -5V, the turn-off threshold voltage was approximately -2V. When a narrower sweeping range was used (+2V - -3V - +2V) threshold voltages of +1.3V and -0.8V were observed. A narrower scan range still (+1V - -2V - +1V) produced threshold voltages of +1V and -0.1V. While too much value should not be attributed to results such as these, they serve to illustrate the volatile nature of NW FET devices when allowed to rest in air for some time.

However, it has been found that by storing devices under a moderate vacuum it is possible to prolong the 'life' of a device for a number of months. It has also been shown possible to renew NW devices by carrying out a short annealing process at a moderate temperature and low vacuum pressure (60 minutes at 60°C, 10^{-6} mbar). It is presumed that this process removes adsorbed water molecules from the surface of the nanowire devices, and also the dielectric surface.

Due to the large number of devices on a single substrate (as shown previously in figure 2.9), it is possible to probe a large number of devices within a small region of substrate, meaning that each device should have been created in near identical conditions (temperature, carrier gas flow, etc.). With this in mind, it is perhaps surprising to see the large variation in both device appearance and characteristics between adjacent devices, within 1 mm of each other. In some cases, there appears to be a dense mass of tangled wires, whereas is other regions there is a very sparse distribution of wires, barely visible under an optical microscope. Devices representing all types of distribution are probed.

Initially we consider the characteristics of a single NW FET, in comparison with a thin film transistor, enabling the key differences to be understood. Figure 5.19a shows a transfer curve of a typical NW FET measured in air shortly after the device had been fabricated (i.e. with limited exposure to oxygen), while 5.19b shows the output curve of the same device. The channel dimensions, as defined by the separation of the electrical contacts, are width = 500 μm and length =



(a) Transfer curve (V_D=-10V) **(b)** Output curve

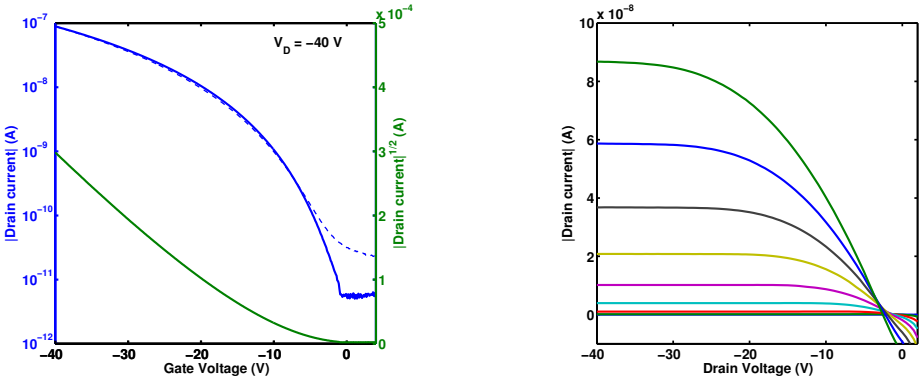
Figure 5.19: Electrical characteristics of CuPc nanowire field effect transistor. Channel width 500μm, length 50μm

50 μm. The substrate used is highly doped silicon, with a 300 nm SiO_2 dielectric layer prepared by thermal oxidation, and cleaned with both solvents and oxygen plasma before NW deposition.

By way of comparison, figure 5.20a shows a transfer curve of a typical TFT measured in air shortly after the device had been fabricated (i.e. with limited exposure to oxygen), while 5.20b shows the equivalent output curve of the same device. The channel dimensions, substrate materials and preparation and measurement conditions are similar for both devices.

As can be seen clearly from the comparative figures, the curve shape in both devices is significantly different. A number of key differences in the overall characteristics are:

- ✓ Voltage ranges used for NW device is far smaller than for TFT,
- ✓ fast transition between 'off' and 'on' states for NW device, far more gradual transition for TFT,
- ✓ straight linear curve shape above |threshold voltage| in NW device, gradual curve for TFT,
- ✓ larger change in current between 'off' state and 'on' state for NW device,



(a) Transfer curve (V_D=-40V) **(b)** Output curve

Figure 5.20: Electrical characteristics of CuPc thin film transistor. Channel width 500μm, length 50μm

✓ saturation behaviour reached at far smaller voltage for NW device,

✗ current noise/instability visible in NW output curve,

✗ larger 'on' current values for TFT,

where ✓ represents advantages for NW devices and ✗ represents preferred behaviour for TFTs over NW FETs.

It is these key differences which are at first striking when viewing the behaviour of these devices. We will next try to understand them in more detail, by studying the variation across many devices.

5.3.3.3 Individual device behaviour

Low resolution SEM images were taken of an array of devices spanning a chip, with source and drain contacts having been pre-defined, as discussed elsewhere (section 2.4.1.2). Figure 5.21 shows these images, arranged as the devices are found on the chip on which they were fabricated, with eight devices each of various channel lengths. It is clear to see how varied the coverage of CuPc is between adjacent devices. Having characterised each device electrically it is possible to attribute these electrical results to each individual device and its physical structure.

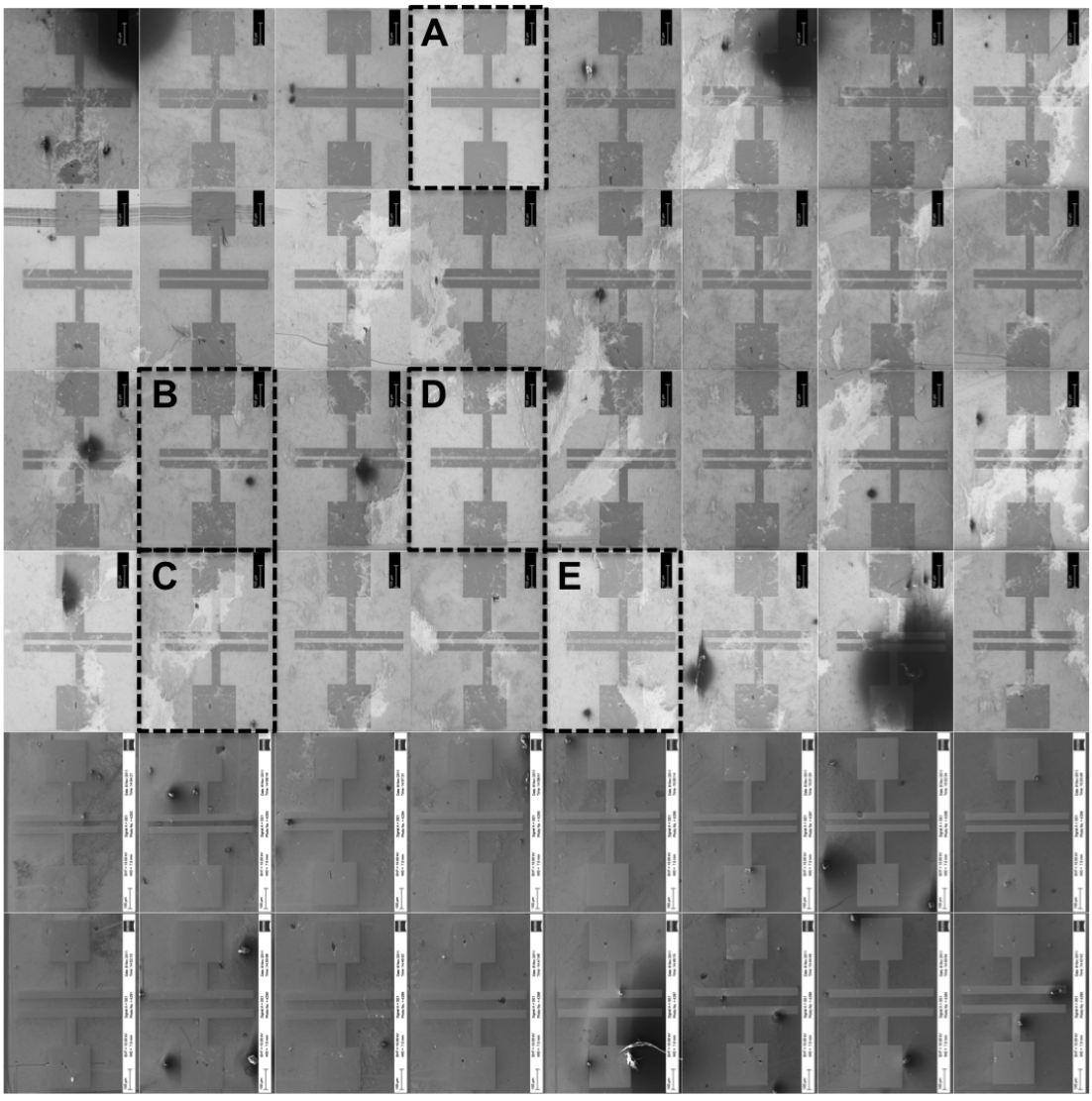


Figure 5.21: SEM images of many NW TFTs. Devices 'A', 'B', 'C', 'D' and 'E' are highlighted.

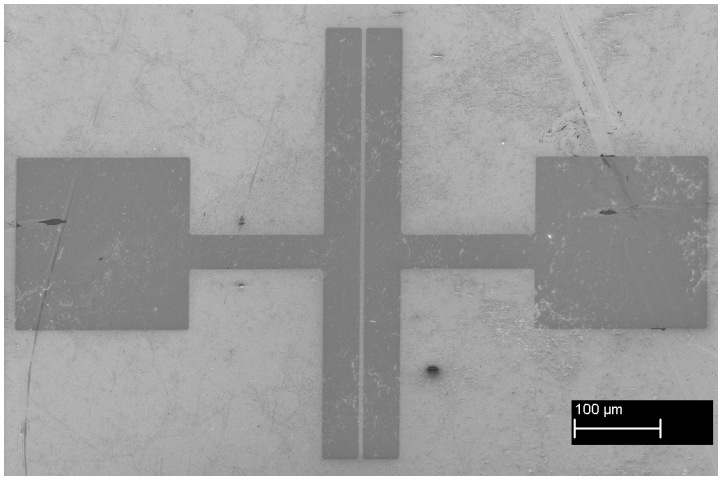
Highlighted in figure 5.21 are a number of devices we will examine in greater detail. Larger images of the devices labelled as 'A', 'B' and 'C' in figure 5.21 are reproduced in figure 5.22. It can be seen that device 'A' shows very little evidence of CuPc on the surface. Device 'B' shows some regions in which a larger number of NWs are present, while device 'C' is largely covered in NWs. On a first inspection, one would expect that device 'C' would behave significantly differently from either devices 'A' or 'B', with a significant proportion of the channel region covered in a thick band of CuPc NWs. Transfer and output characteristics for the three devices shown are plotted in figure 5.23.

Similar device characteristics and performance are shown by devices 'A' and 'B' (figures 5.23 (a-b) and (c-d)) which have channel widths of 500 μm and lengths of 5 and 15 μm respectively. The sub-threshold slope and turn on voltage are similar, with field effect mobility estimated to be $\approx$0.6-0.8 $\times 10^{-3} cm^2/Vs$.

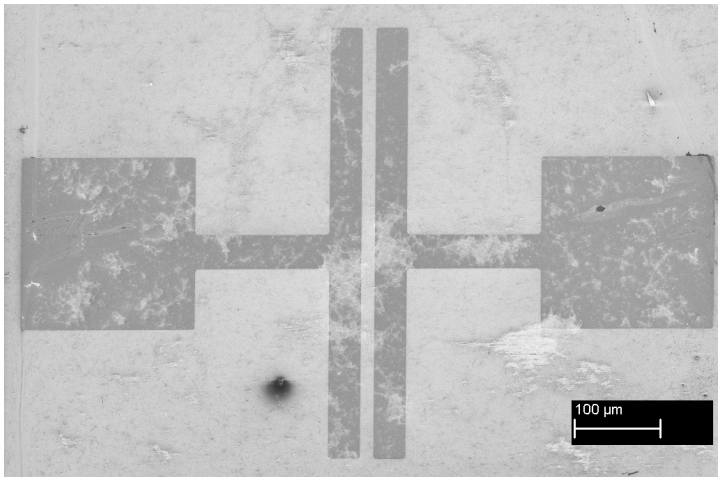
A significant difference is seen when considering the characteristics of devices 'A' and 'B' with with those of device 'C' (figures 5.23(e-f)). As can be seen from the transfer curve the turn-on region is far less abrupt than for the other devices, with a gradual transition seen between the off and on states, over several volts of gate bias. However, once biased above threshold voltage (-2.3 V) the estimated mobility is higher than the other devices, while in other respects, such as the good saturation behaviour and on/off ratio, the device performs well.

As can be seen from the SEM images of all three devices (figure 5.22), device 'C' contains a high proportion of densely packed NWs, whereas 'B' contains only a small region where this is the case. Device 'A' contains very few regions in which a dense mat of wires is visible in SEM images.

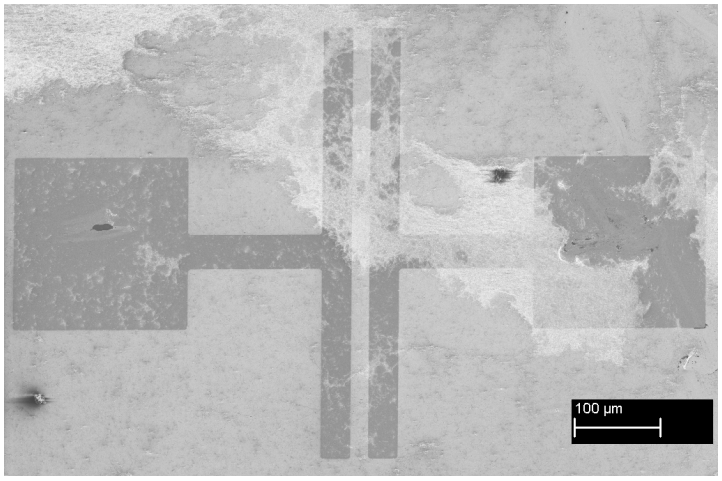
It can be imagined that a device like 'A' with a small density of wires will have a far smaller number of conducting paths between source and drain than a device more similar to 'C'. In fact, the mass of wires seen in 'C' is more similar to a continuous film than a collection of discrete wires. The effective 'blurring' in the characteristics seen in figure 5.23e when compared to 5.23a can possibly be explained by the fact that rather than a small number of parallel channels functioning more or less with the same characteristics, there are an extremely large number of channels, all operating with slightly different turn-on voltages, and effective channel dimensions. In fact, due to the nature of the bundles of



(a) Device 'A'

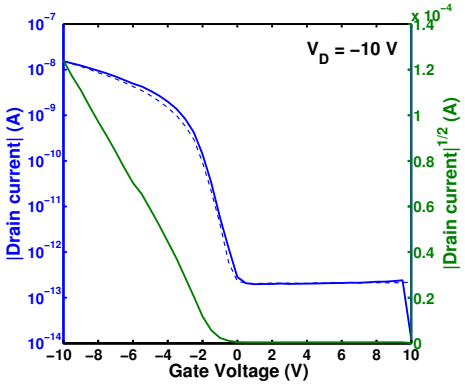


(b) Device 'B'

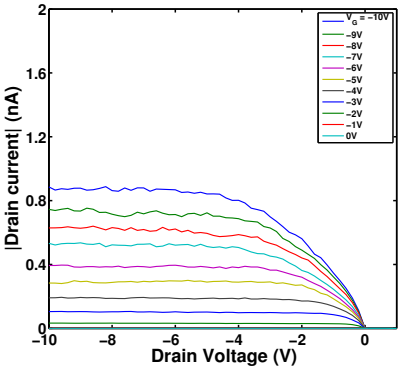


(c) Device 'C'

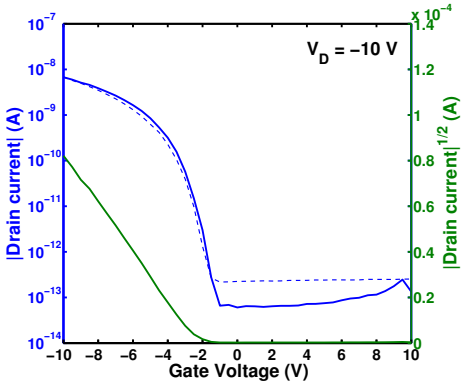
Figure 5.22: SEM images of several NW TFTs



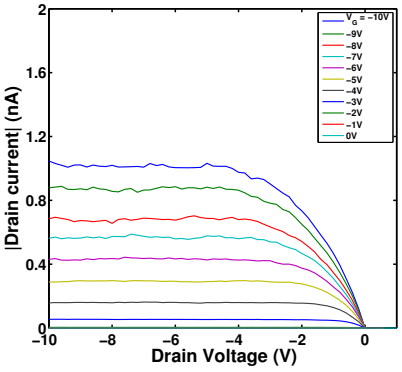
(a) Transfer curve device 'A'



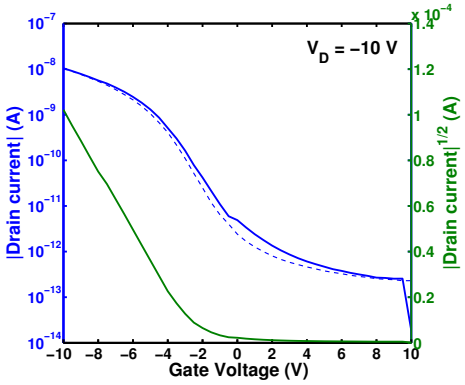
(b) Output curve device 'A'



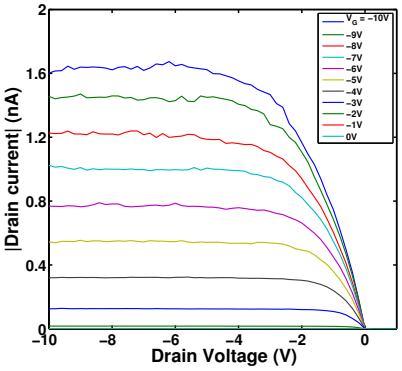
(c) Transfer curve device 'B'



(d) Output curve device 'B'

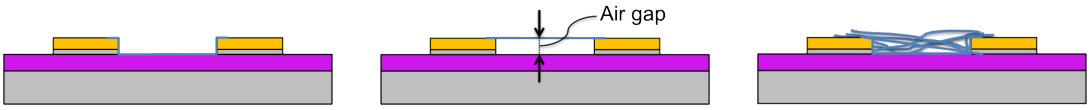


(e) Transfer curve device 'C'



(f) Output curve device 'C'

Figure 5.23: TFT characteristics of several NW TFTs



(a) Ideal single NW device

(b) Single NW device with variable air gap

(c) NW device with many wires

Figure 5.24: Schematic illustrations of NW devices with wires in contact and separated from the dielectric surface.

wire known to comprise the NW mat regions, it is highly likely that a significant amount of the semiconducting material which connects the source and drain contact is not in direct contact with the dielectric surface. It is also highly probably that the length of each 'channel' formed amongst the many will vary significantly from the direct distance between contacts.

Figure 5.24 illustrates the possible configurations of a nanowire device. In figure 5.24a a single wire is shown in contact with the dielectric, an ideal device. In figure 5.24b an idealised device is shown, now with a single nanowire effectively suspended between raised contacts. In a real device, it is likely that portions of wires are raised from the surface, while other portions remain in contact with the surface as no wire is likely to remain completely unsupported along its entire length. A device with many wires is shown schematically in figure 5.24c, in which some many wires are both partially in contact (air gap = 0 nm) and partially raised (air gap > 0 nm). This represents a more realistic device, however, the simplified representations are considered first to understand the impact of some degree of separation between the nanowire and dielectric. The degree of coupling between NWs and dielectrics has been recognized as a significant problem in the field of NW TFTs [119].

It will be appreciated that if a single wire device were to have an air-gap between the semiconductor and dielectric, then the capacitance of that wire, with respect to the gate will be reduced in accordance with the equation below:

$$\frac{1}{C_{tot}} = \frac{1}{C_{ox}} + \frac{1}{C_{air}} \tag{5.1}$$

Where C_{tot} is the total capacitance, C_{ox} is the gate dielectric capacitance and C_{air} is the capacitance of the air gap, and each component capacitance is related to

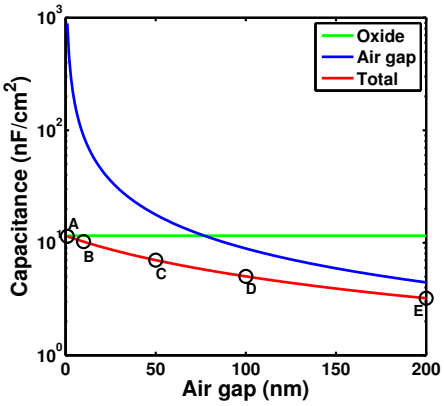
the dielectric constant of the dielectric medium (ϵ_r), permittivity of free space ϵ_0, area (A) and separation (d) according to the expression $C = \frac{\epsilon_0 \epsilon_r A}{d}$. Furthermore, substituting this expression for each component capacitance in equation 5.1 and rearranging, the total capacitance will depend on the separation as described in equation 5.2:

$$C_{tot} = \frac{\epsilon_0 \epsilon_r A}{\epsilon_r d_{ox} + d_{air}} \tag{5.2}$$

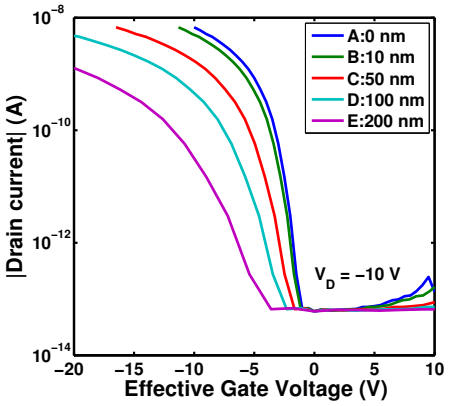
The resulting reduction in capacitance could dramatically affect the current voltage characteristics. As can be seen from the modelled device characteristics in figure 5.25aa, the introduction of an air gap of just 100 nm can be responsible for a dramatic reduction in capacitance of over 50%. The change in capacitance will in effect stretch the transfer curve along the voltage axis, as illustrated in figures 5.25b and 5.25c, with gaps of 0, 10, 50, 100 and 200 nm all considered. This will alter the device characteristics significantly, by increasing threshold voltage, reducing sub-threshold slope.

Figure 5.25d further shows the effect of an air gap on extracted field effect mobility. While the initial device's mobility peaks at $\approx 0.75 \times 10^{-3} cm^2/Vs$, if an air gap is introduced, the apparent mobility would fall significantly, to as low as $0.06 \times 10^{-3} cm^2/Vs$ with a gap of 200 nm. While it is not suggested that this situation is the case with many of our tested devices, it must be acknowledged that a device geometry which introduces the potential for variation in an out-of-plane 3^{rd} dimension, may lead to extracted mobilities and sub-threshold slopes which are far below the intrinsic values supported by the materials investigated.

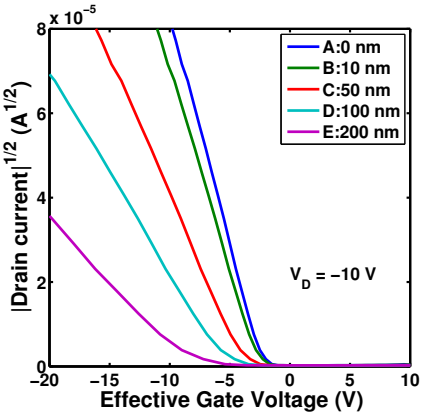
In this simulation, a real transfer curve (device 'B') is altered to examine the effect of introducing an air-gap between wires and the dielectric surface. While any real device is unlikely to consist of wires either entirely in contact with the surface, or entirely suspended at a fixed distance, a mixture of states would lead to some distortion to the observed transfer curve, and to a likely underestimate of the device performance due the charge sheet approximation used to calculate mobility.



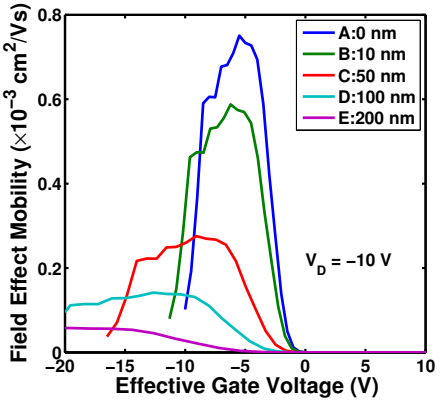
(a) Capacitance variation with air gap



(b) Estimated transfer curve variation with air gap



(c) Estimated transfer curve variation with air gap



(d) Estimated mobility variation with air gap

Figure 5.25: The effect of NW suspension on capacitance and transistor characteristics

Parameter		Device			Whole chip	
		A	B	C	Median	MAD[a]
Channel length	(μm)	5	15	20	5–50	5–50
Threshold voltage	(V)	-0.4	-2.3	-2.3	-2.1	0.54
Mobility	$(\times 10^{-3} cm^2/Vs)$	0.6	0.8	1.4	1.2	0.4
Hysteresis	(V)	-0.3	-0.2	-0.1	-0.2	0.1
On/off ratio	$(log_{10} \frac{I_{on}}{I_{off}})$	6.1	5.1	5.7	5.7	0.3
Sub-threshold slope	$(V/decade)$	0.65	0.48	1.59	0.87	0.37

[a] Median absolute deviation (MAD).

Table 5.3: Nanowire field effect transistor parameter summary showing individual devices 'A', 'B' and 'C' and median performance of 33 devices of various geometries.

5.3.4 Statistical Analysis

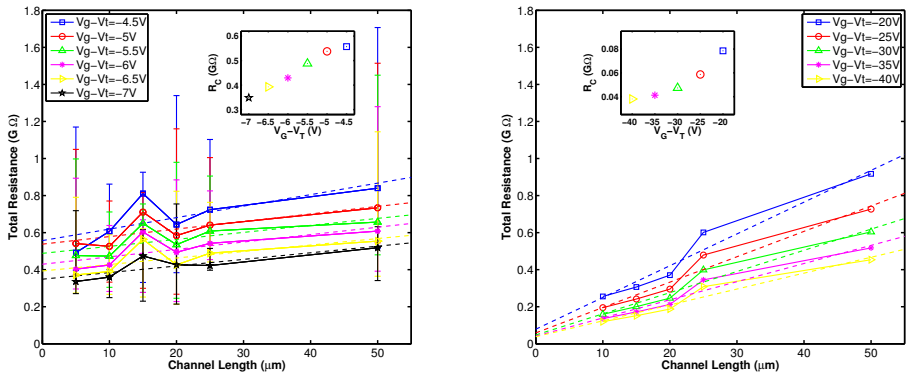
5.3.4.1 Chip wide device comparison

A significant feature of this device architecture is the ability to fabricate many devices in parallel on a single substrate. Discussed above are the characteristics of a few individual devices, but to gain a better understanding of the potential for application it is necessary to consider a larger number of devices. Table 5.3 summarises the extracted parameters of each of the devices discussed above, along with providing equivalent parameters for the large number of devices tested.

While there is significant spread in device characteristics, it is perhaps less than might be expected considering the significant variability in the density of NWs on each device, as seen from SEM images in figure 5.21. The median device threshold voltage is just -2.1 V, with estimated mobility 1.2×10^{-3} cm^2/Vs.

5.3.4.2 Length Dependence

A further observation made possible by the collection of data from a large number of devices, including data from a variety of device geometries, is that of the relationship between channel length and device characteristics. The equations used to extract mobility from terminal measurements initially assume that resistance will scale linearly with device length, or that conductance will be inversely



(a) Nanowire Field Effect Transistors **(b)** Thin Film Transistors

Figure 5.26: The effect of channel length on total resistance.

dependent on length. However, in these nanowire devices, an extremely weak dependence on length is observed. This aspect of performance is illustrated in figure 5.26a in contrast with 5.26b.

For thin film devices fabricated in accordance with the description in section 5.1 it can be seen for a number of devices that there is a strong dependence of the total resistance on channel length, with a best-fit line having a small zero-length intercept, as plotted in the inset figure. However, in the case of NW devices, while a significant spread of device behaviour is observed, a plot of median total resistance for each channel length results in some length dependence, but where the zero-length intercept is significant when compared to the length dependent component of resistance.

By considering these results in terms of device behaviour, as described by section 2.3.1.4, it is possible to extract an effective contact resistance for each set of devices. By calculating the ratio of the length dependence of the total resistance ($\frac{\delta R_{TOT}}{\delta L}$) to the zero-length offset (R_C), we can further extract a length term that describes the equivalent length device which is equivalent to the contact resistance, ΔL.

It can be seen from table 5.4 that the contact resistance in TFTs is equivalent to a channel length of $\approx 4.3\ \mu m$, whereas the NW FETs equivalent length is $\approx 115.7\ \mu m$. This result suggests that while in film devices the contact resistance is not hugely significant, in nanowire devices it can dominate the behaviour. It is

NW FET			TFT		
$V_G - V_T$	R_C	ΔL	$V_G - V_T$	R_C	ΔL
(V)	$G\Omega$	μm	(V)	$G\Omega$	μm
-5.0	0.538	132.09	-20	0.079	4.58
-5.5	0.488	129.27	-25	0.059	4.28
-6.0	0.429	107.34	-30	0.047	4.14
-6.5	0.393	112.26	-35	0.041	4.21
-7.0	0.349	97.68	-40	0.038	4.44

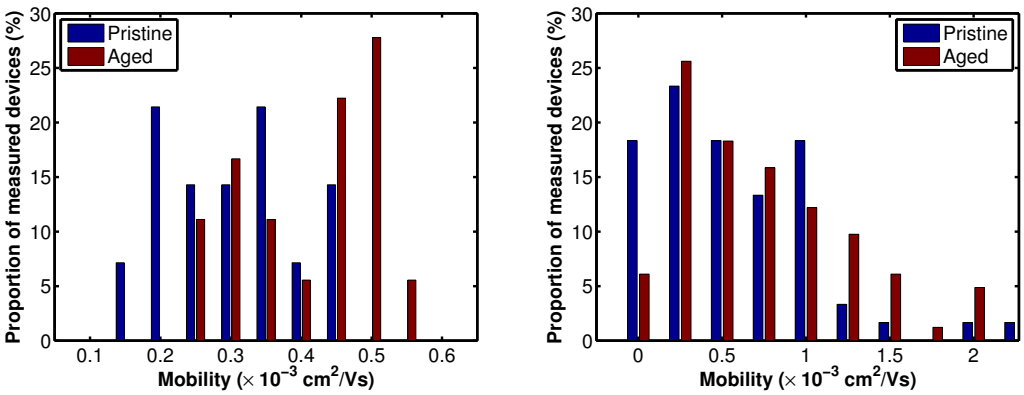
Table 5.4: Contact resistance extraction in thin film and nanowire field effect transistors.

clear that the contribution to resistance from carrier injection into NW devices is in the region of an order of magnitude larger than the contribution from the smallest channel length (5 μm), whereas for film devices, while still significant, this value is closer to being of approximately the same magnitude as that of the shorter devices, and an order of magnitude smaller than the contribution from the long channel (50 μm) devices.

What is also apparent from the large number of results collected is that the variation in NW device behaviour does not have a strong dependence on channel length. This aspect has not been studied previously, with several studies discussing multi or single wire devices, but none recognizing that the channel length itself is an important aspect to consider. If only a single channel length is studied, the fact that the resistance is approximately length invariant cannot be detected.

5.3.5 Air Stability

A further aspect of device performance to consider is that of air stability. While a-Si:H TFTs are a well established technology, one of the key challenges facing the adopters of OTFTs and other alternative organic electronic devices are the problems associated with extended exposure to ambient conditions. The presence of oxygen, nitrous oxide [120, 121, 122] and other oxidising agents has been shown to have a significant effect on many organic electronic devices. We have examined a number of devices after prolonged storage in an ambient environment



(a) Thin Film Transistors **(b)** Nanowire Field Effect Transistors

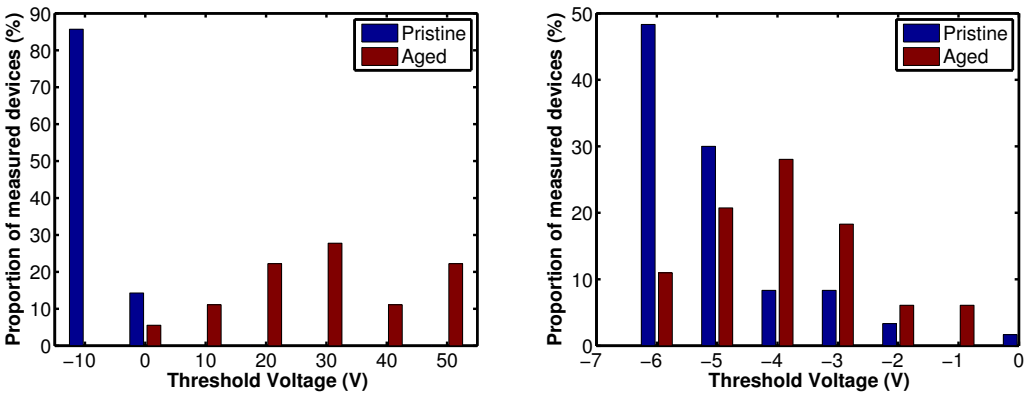
Figure 5.27: Variation in field effect mobility of pristine and aged transistors.

to explore any degradation associated with storage. To provide adequate basis for comparison, equivalent measurements were made on thin film devices having also been stored in similar conditions for a similar duration of time.

It must be noted that earlier measurements presented of NW devices were preformed on devices which had both been stored for a period of approximately 6 months, and separated from one another by a process of scratching along the surface of the chip with a fine probe tip. Comparative results here are presented of devices which have not been 'separated', both before and after storage, allowing a direct comparison to be made. It is further suggested that an improvement in 'pristine' device performance would be observed if a similar process was carried out at the time of fabrication before first the devices were characterised.

As can be seen from the comparative plots of figure 5.27, there is a wide distribution of extracted mobility values both seen in pristine devices and those aged by $\approx$ 6 months storage. A similar characteristic is true for both thin film devices, as represented by figure 5.27a, and NW devices, shown in figure 5.27b. However, it is noticeable that a majority of the NW devices, both pristine and aged have a mobility above those seen in continuous films. Furthermore, the variation between both sets of data is far smaller in the case of NWs when compared to films.

A similar comparison is made in figure 5.28, now considering the threshold voltage change in both sets of devices over the same storage period. Again figure



(a) Thin Film Transistors **(b)** Nanowire Field Effect Transistors

Figure 5.28: Variation in threshold voltage of pristine and aged transistors.

Device	Parameter	Pristine		Aged		Aged (sc)	
		Median	MAD	Median	MAD	Median	MAD
NW	$\mu(\times 10^{-3} cm^2/Vs)$	0.48	(0.38)	0.62	(0.43)	1.12	(0.69)
	$V_T(V)$	-5.5	(0.9)	-3.8	(1.6)	-2.7	(0.8)
TFT	$\mu(\times 10^{-3} cm^2/Vs)$	0.31	(0.08)	0.44	(0.08)	-	-
	$V_T(V)$	-10.0	(2.7)	33.0	(12.1)	-	-

Table 5.5: Variation in threshold voltage (V_T) and field effect mobility (μ) of pristine and aged transistors. Data also shown for NW devices once they have been isolated from one another by a scratching process.

5.28a shows TFTs, and figure 5.28b NW devices. What is immediately apparent is the degree of variation in the threshold voltage of thin film devices, of which the median value changes from -10V in the pristine state, to ranging widely from 0V to +50V, with a median of 33V. However, NW devices stored for the same period typically show far smaller variation, with a median threshold voltage changing from -5.5 V to -3.8 V, as shown in table 5.5.

This is further illustrated by the plot shown in figure 5.29, which shows the extent to which thin films devices tend to vary over the storage period. In the same time, the performance of NW FETs is far less changed, suggesting a higher degree of stability in an ambient atmosphere, and consequently a high degree of suitability to switching devices which will be operated over an extended time

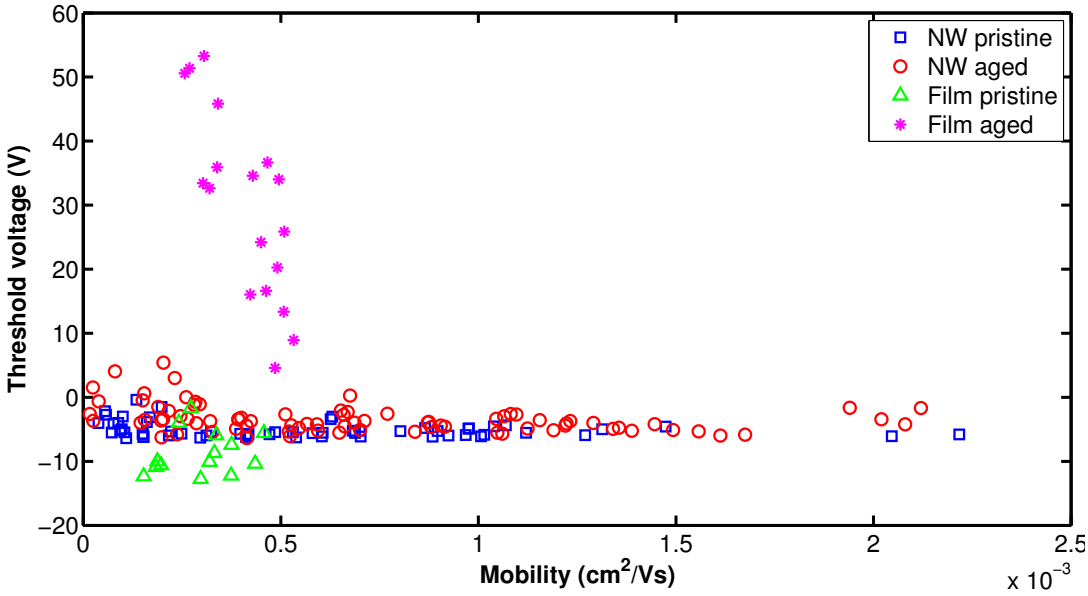


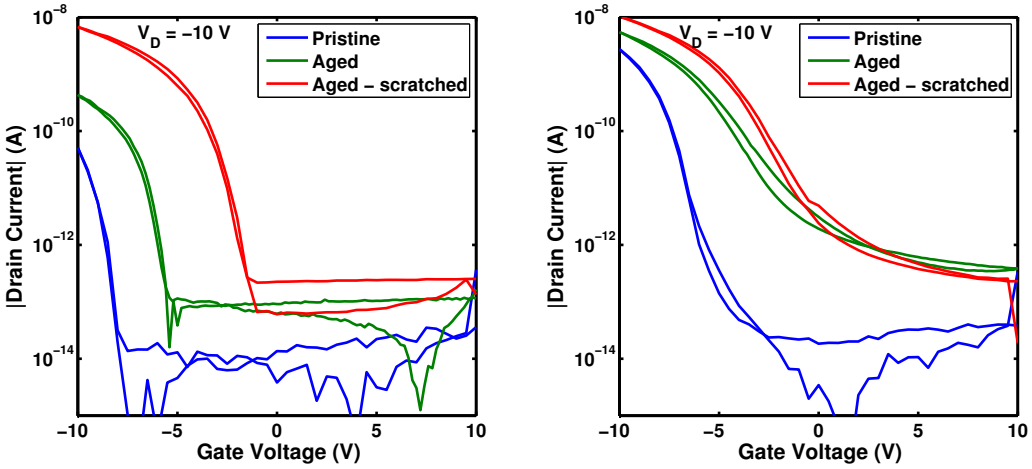
Figure 5.29: Variation in threshold voltage (V_T) and field effect mobility (μ) of pristine and aged transistors.

period requiring minimal encapsulation.

As mentioned above, devices were scratched to separate adjacent devices from one another. The table 5.5 also includes a summary of NW devices which have been separated, which show, on average, an enhancement in mobility of approximately a factor of two. The enhancement brought about by scratching can best be seen with reference to individual device behaviour. Figure 5.30 shows transfer curves measured on pristine devices, devices which were stored in air for 6 months, and then the same devices but having been separated by a scratching process. It can clearly be seen in each case that the threshold voltage has moved towards 0 V, and also that the on-current has improved with both storage and scratching.

5.3.6 Image Analysis

Using techniques such as SEM and AFM it is possible to take high resolution images of regions of NW devices, allowing access to information about the arrangement of wires unobtainable from an electrical measurement or optical mi-



(a) Device 'B' **(b)** Device 'C'

Figure 5.30: Variation in transfer characteristics of pristine, aged and scratched transistors.

crograph. While impractical to examine every device at this level of detail, it can provide an invaluable guide to characteristics of many devices if it is shown that there is some similarity between the arrangement of wires between distinct devices. In this way, effort invested in the analysis of a small number of devices can be applied to a larger set of data for the purpose of understanding the behaviour of the group of devices.

Figure 5.21 showed a large number of devices tested, but we will now look in more detail at a small number of devices in particular. Device 'D' in 5.21 has a contact separation of 15 μm and contact width of 500 μm and is shown in higher resolution in figure 5.31. However, by using a higher magnification it is possible to resolve to the level of individual nanowires. Figure 5.31 shows a series of sub-images taken from device D, as illustrated. It is now possible to trace individual wires from one contact region to the other. For example, it can be seen that in sub-images (g) and (h) that a line can be drawn from one boundary to the other without crossing a single nanowire. It is obviously the case that wires are not evenly distributed at this length scale, and as such, the effective channel width is far smaller than that estimated by merely considering the width of the source

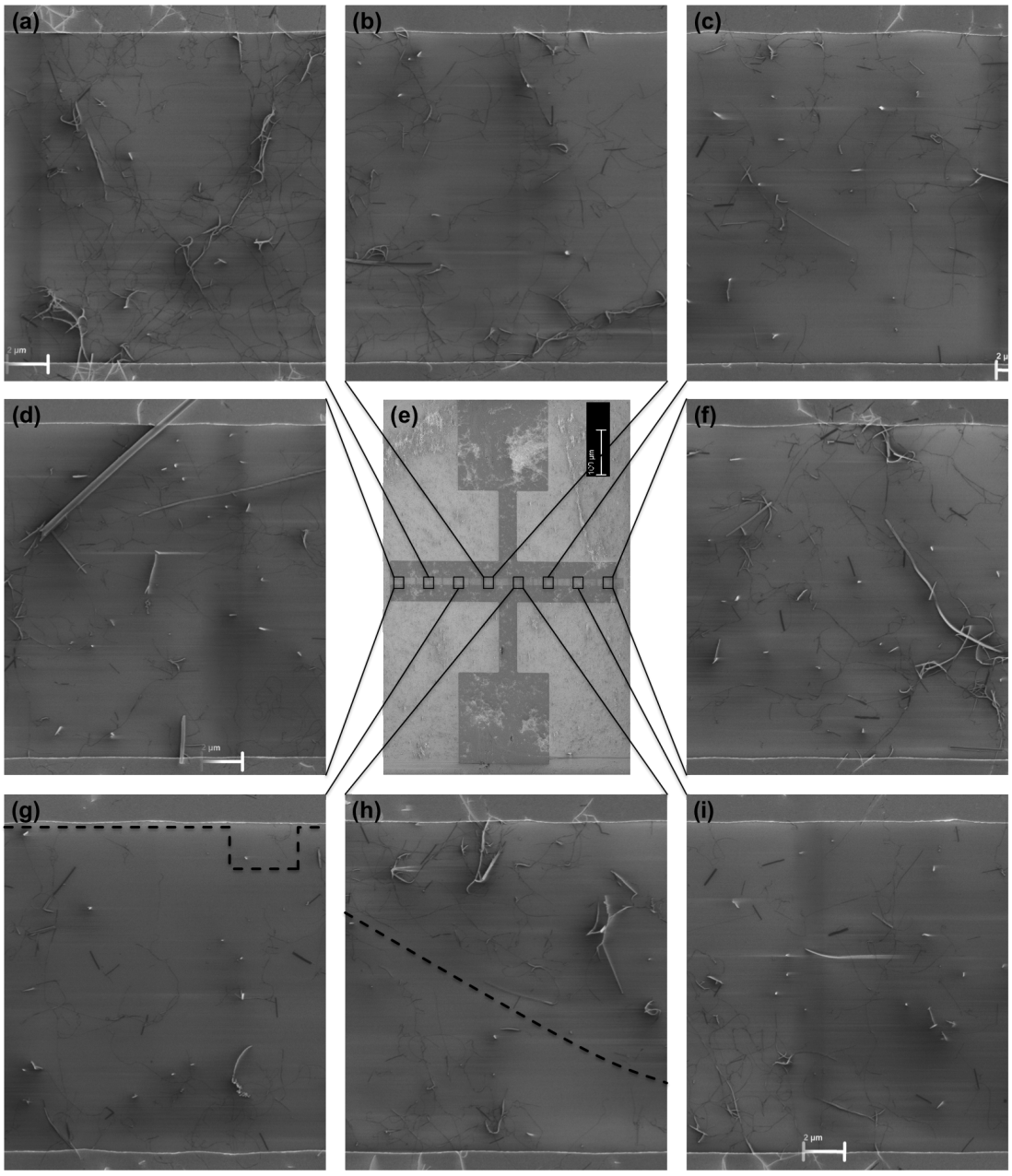


Figure 5.31: SEM images and sub-images of NW TFT device 'D'

and drain contacts.

While it is obvious to the naked eye that not all of the area between contact is covered in wires, this proves less straight forward to assess in a quantitative way. Here it is necessary to define the term 'coverage' as meaning the proportion of the channel region, as defined by the contact separation and width, which is covered by semiconductor. For example, a thin film transistor, as discussed in previous chapters will have a coverage of 100%, whereas our devices, as illustrated in figure 5.31, have a far lower proportion of the area covered. Further to using a measure of 'coverage' it is also necessary when calculating TFT parameters to have a measure of the channel length and width. We will use the terms *effective length* (L_{eff}) and *effective width* (W_{eff}) for this purpose. Again referring to a fully covered device, the length and width are solely defined by the dimensions of the metal contacts.

A number of strategies for extracting the effective channel dimensions were considered:

(a) Full wire detection and counting, pixel by pixel.

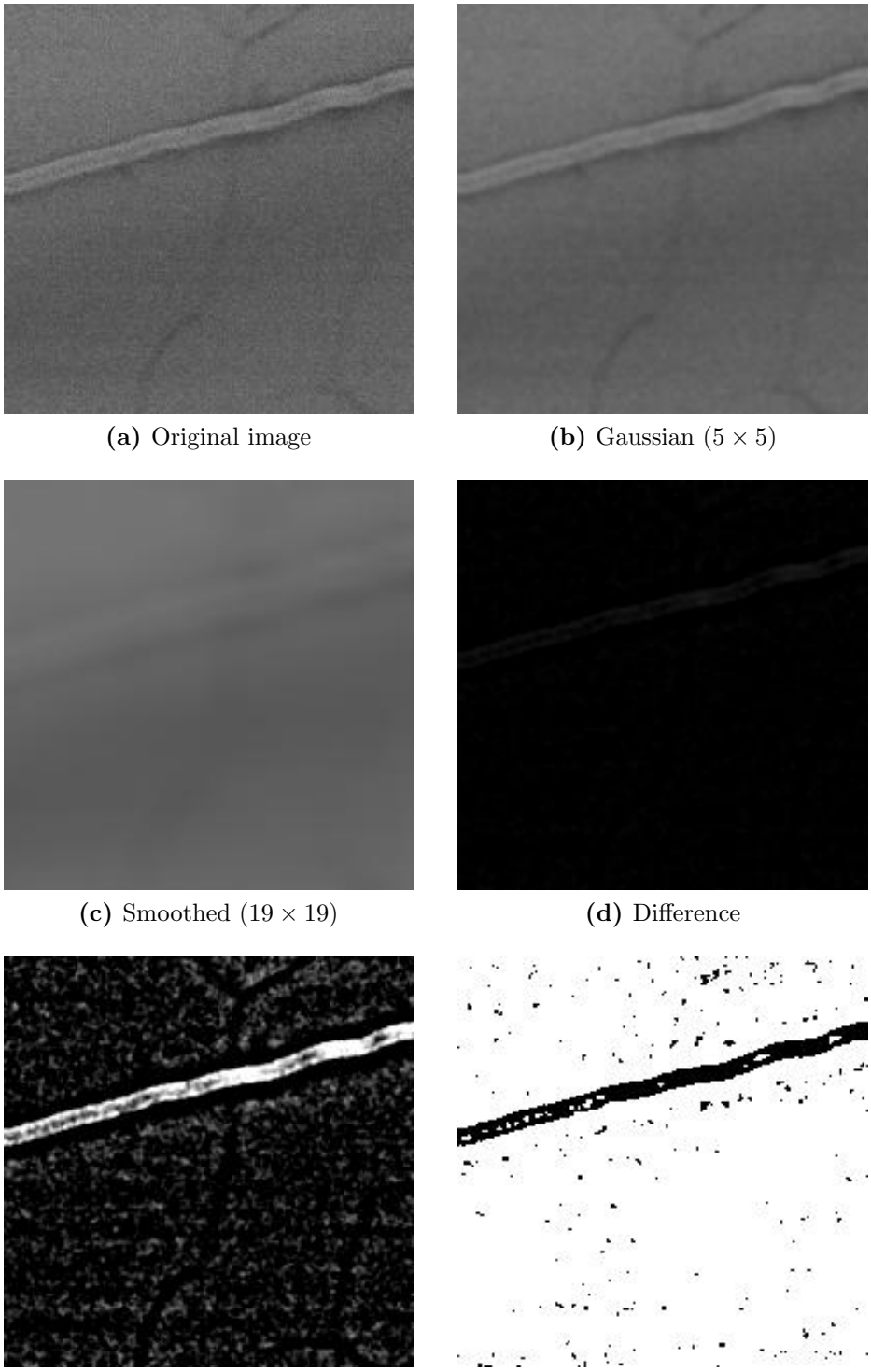
(b) Regional sampling and extrapolation.

(c) Line by line sampling and extrapolation.

5.3.6.1 Full wire detection

A large number of overlapping high resolution SEM images were obtained of a single NW device, and image stitching performed using DoubleTake[1], a freely available image processing tool. The combined image was cropped using Gimp[2], yielding a 'tif' greyscale image which was imported into a MATLAB[3] work environment. To allow more efficient optimisation of processing techniques, a number of small (200×200 pixel) sub-images were selected within the larger (2067×48632 pixel) image, each representing a distinct region. The particular regions analysed are, for the time being, identified as containing either thin wires or thick wires, where the distinction is made at a wire width of a few 10s of nm.

[1]DoubleTake, version 2.2.6 (682), from Echo One (http://echoone.com)
[2]GIMP 2.6.11, GNU Image Manipulation Program, www.gimp.org
[3]MATLAB 7.11.0.584 (R2010b), from MathWorks



(a) Original image

(b) Gaussian (5×5)

(c) Smoothed (19×19)

(d) Difference

(e) Intensity adjusted

(f) Threshold filtered

Figure 5.32: Various filters applied to SEM image of 'thick' CuPc wire (SEM image 200x200 pixels, 2.2μm $\times$ 2.2μm)

For a single thick wire, such as that clearly visible in figure 5.32a is relatively simple to enhance the image contrast sufficiently to obtain a binary mask covering just the location of the wire in question. This was carried out in a series of steps. Firstly, the image is smoothed by a small Gaussian filter, removing some pixel noise from the image, while preserving all essential features. The filter used for this functions a Gaussian distribution, using a 5×5 matrix, with a standard deviation of $\frac{5}{6}$:

$$\begin{bmatrix} 0.0007 & 0.0063 & 0.0129 & 0.0063 & 0.0007 \\ 0.0063 & 0.0545 & 0.1119 & 0.0545 & 0.0063 \\ 0.0129 & 0.1119 & 0.2299 & 0.1119 & 0.0129 \\ 0.0063 & 0.0545 & 0.1119 & 0.0545 & 0.0063 \\ 0.0007 & 0.0063 & 0.0129 & 0.0063 & 0.0007 \end{bmatrix} \tag{5.3}$$

A further transformation was performed on the image to carry out a smoothing function, by averaging each pixel brightness over its local region. The matrix used to perform this was simply a matrix of 'ones', scaled such that the overall image intensity remains unchanged. While it was decided to use a large (19×19) matrix for the actual smoothing operation, to allow subtraction of the local background, here shown is a similar but simpler 5×5 matrix:

$$\begin{bmatrix} 0.04 & 0.04 & 0.04 & 0.04 & 0.04 \\ 0.04 & 0.04 & 0.04 & 0.04 & 0.04 \\ 0.04 & 0.04 & 0.04 & 0.04 & 0.04 \\ 0.04 & 0.04 & 0.04 & 0.04 & 0.04 \\ 0.04 & 0.04 & 0.04 & 0.04 & 0.04 \end{bmatrix} \tag{5.4}$$

The filtered outputs of both of these transformations are shown in figures 5.32b and 5.32c.

Once both filters have been applied, the smoothed image is subtracted from the Gaussian filtered image, resulting in a difference image. This result is a greyscale image with extremely low values, and as such must be contrast adjusted before being visible. To perform this function, the image intensity is modified such that 1% of pixels are saturated at high intensity (255) and similarly also at low intensity (0). This difference image, and the intensity adjusted difference

image are shown in figure 5.32e.

Finally, it is possible to create a binary mask describing just the wire by using a simple threshold of the intensity values contained within the adjusted difference image. Figure 5.32f shows the binary image creased when a threshold of 95 is used, and effectively inverts the original feature.

Having seen a simple procedure to identify and extract the shape of a wire from an SEM image, we apply the same technique to a rather different image, this time one of several finer wires, as shown in figure 5.33a.

Figure 5.33 shows the same filtered and summed images as were shown for the thick wire, yielding a far less obvious output. In this case, a different approach must be tried to extract the finer wires, as they are both less well resolved, and shown in lower intensity, rather than higher intensity perturbations from the background.

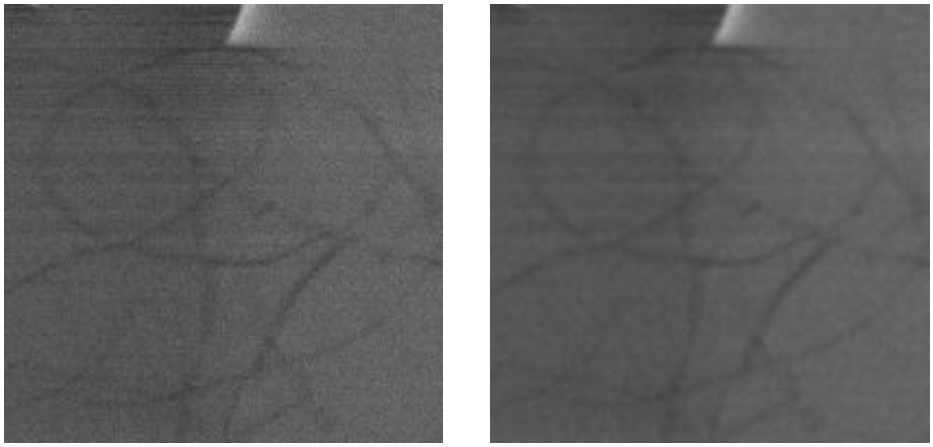
Finally, a threshold is applied, revealing just regions of the image that are covered in fine wires. However, as can be seen from figure 5.33f the wires are incomplete due to poor contrast resolution. Also, there is still some degree of noise remaining in the inter-wire regions. Further work is required to attain a more complete wire mask.

5.3.6.2 Regional Sampling

As can be seen from figure 5.31 there is a high degree of variation between different regions of one device. By sampling a small number of isolated regions, it was not considered likely that a true representation of the full device would be made up. Each device has a unique layout, which may vary significantly from one region to another, with a low degree of self-similarity between different length scales. Bearing this in mind, it would be possible to randomly sample a device and yet still avoid critical features, which may make up an extremely small percentage of the overall area.

5.3.6.3 Line By Line

It will be appreciated that analysing a complete high resolution image of the sort discussed (48000×1500 pixels) could take some considerable computing effort.

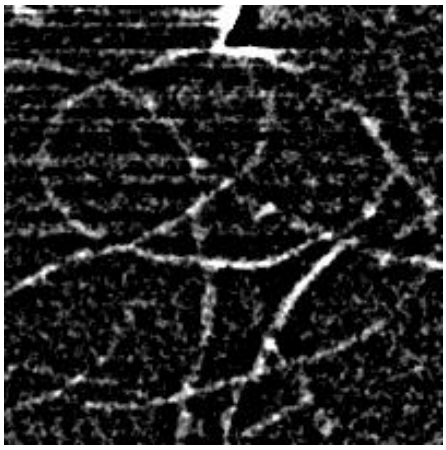


(a) Original image (5×5)

(b) Gaussian (5×5)

(c) Smoothed (19×19)

(d) Difference



(e) Intensity adjusted

(f) Threshold filtered

Figure 5.33: Various filters applied to SEM image of 'thin' wires. (SEM image 200x200 pixels, 2.2μm $\times$ 2.2μm)

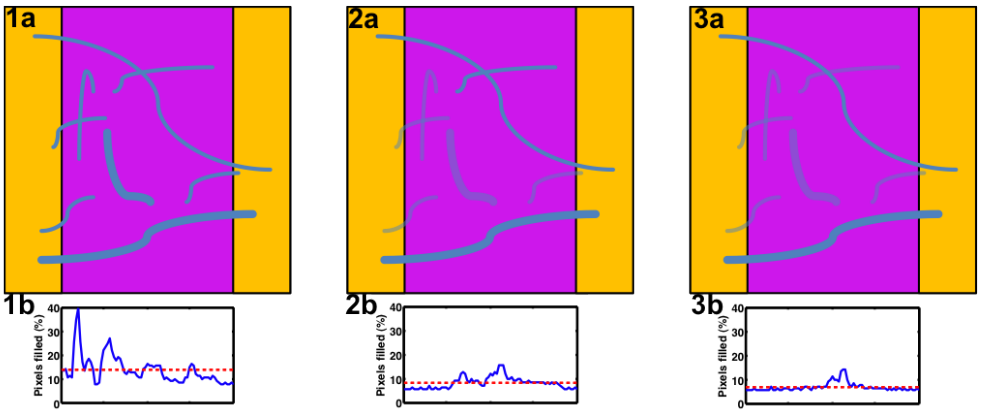


Figure 5.34: Schematic illustration of various approaches to estimating the true transistor channel dimensions. (1a) All wires considered, (2a) Unconnected wires excluded, (3a) Only fully connected wires considered, (1b, 2b, 3b) Line by line channel width estimation corresponding to (1a, 2a, 3a) respectively. Solid blue line represents instantaneous channel width. Dotted red line represents full device average for each channel region. Wires shown faintly in 2a and 3a are excluded from counting algorithm.

Further still, applying the technique to future devices would also incur a high computational cost. While understanding the true geometry of a NW device channel is a possibly interesting goal, it is not necessary to understanding the behaviour of a device. In fact, it is possible that by considering the entire device, one could be misled as to the true behaviour of the wires as semiconductors. Considering the schematic illustrations of figure 5.34, it can be seen that if all wires in the device are analysed, leading to % coverage figure, then this number will hugely overestimate the number of wires contributing to the conduction. However, the total number of wires provides a useful upper bound for the number of contributing wires.

If, on the other hand, a line by line approach is taken, with the number of pixels filled within each line of an image (as in figure 5.34 part 1b) , then the minimum line value can be taken to be the limiting effective channel width (W_{eff}). This too is an over-estimate of the true W_{eff}, but again provides an upper-bound, albeit a more accurate one.

A more accurate measure still would be to perform the above steps, but first exclude any wires which are not connected, by themselves, or through other

	All	Connected	Essential
Full image total (%)	14.0 (244)	8.3 (146)	6.9 (122)
Line-by-line maximum (%)	40.0 (700)	15.7 (275)	14.2 (250)
Line-by-line minimum (%)	7.9 (138)	5.7 (100)	5.7 (100)

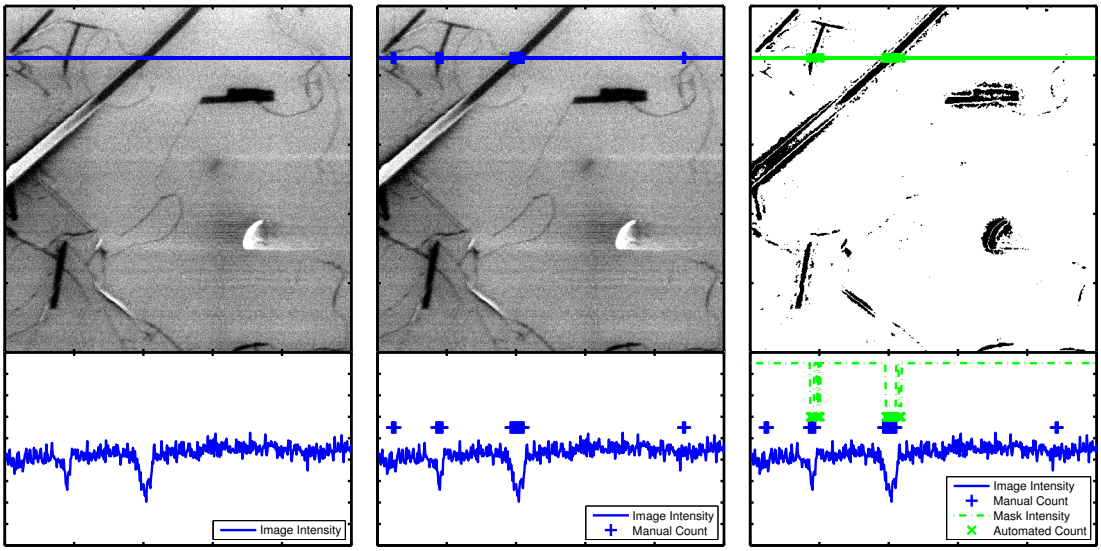
Table 5.6: Extraction of effective channel width from modelled SEM images. Percentage of minimum (limiting) value in brackets.

wires, to both contacts. This filter has been applied in figure 5.34 part 2a, with the corresponding line by line pixel sum in part 2b.

Furthermore, if the full image mask created by the process described above is considered line-by-line, with some consideration being given to the correlation between adjacent lines, then a highly accurate measure of current pathways could be achieved. Rather than just excluding unconnected wires, it would be necessary to exclude all non-essential branches from the calculation. This filter has also been applied to the illustrative image of figure 5.34, and is shown in part 3a. The line by line pixel summary is shown in part 3b, showing the lowest percentage pixel count of all devices.

A summary of the results of these extraction methods, as applied to the models images of figure 5.34 is shown in table 5.6. This shows just how significantly counting each wire in an image can over-estimate the real channel width. In the case where all wires are counted, a 'fill factor' of 14% is observed, whereas the likely limiting channel width is a line in which the fill factor is 5.7%. It can also be seen how significant an error can be achieved by attempted a line-by-line analysis. In the example given, the maximum channel width observed by this method would be seven times the real limiting width value. The minimum line-by-line value for the unfiltered image appears to be a reasonably good estimate though, in this illustration, with an estimate that is 138% of the true minimum.

Discussed above are the results of some image modelling, used to develop the tools for application to SEM images of nanowire transistors. High resolution images, of which segments were shown in figure 5.31, are enhanced as described above, to improve the contrast of features as far as possible. Once this has been done, segments of the image were inspected one by one, with a sampling line projected along a particular row of pixels. An image intensity line scan was also



(a) Initial image **(b)** Manual extraction **(c)** Automated extraction

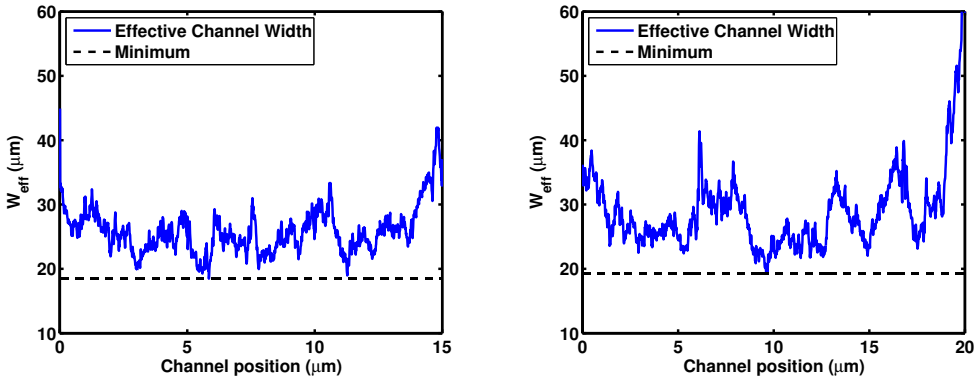
Figure 5.35: Manual and automated wire detection algorithm applied to high resolution SEM image of device 'D'.

displayed, so as to be aligned with the image, allowing manual inspection to be carried out, and an assessment made at every point across the width of an entire device, as to whether there was a wire present at that point. A typical image used for this manual counting task is shown in figure 5.35. Figure 5.35a illustrates the initial image, with intensity line scan below, while figure 5.35b shows the image with detected wires indicated by crosses.

Once a single line scan (≈48000 pixels) had been examined, the total number of pixels was counted, and used to 'tune' the thresholding step of the process described in figures 5.32 and 5.33, ensuring that the total number of pixels detected in the same row would match that counted manually.

Following this, the threshold value was applied to the entire image, resulting in output images, of which a section is shown in figure 5.35c. While it is acknowledged that much of the fine detail is lost, on average, the correct number of pixels have been reproduced, with some small features being reduced in size and larger features over-estimated.

It is now possible to examine, line by line, the entire image generated to assess



(a) Device 'D' **(b)** Device 'E'

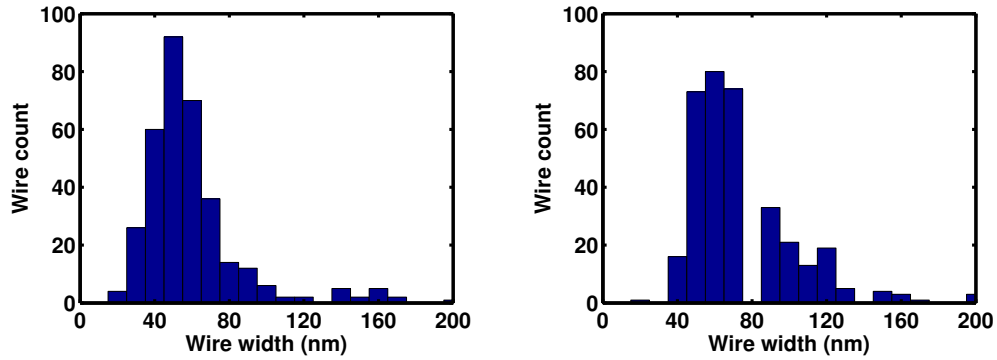
Figure 5.36: Plots showing maximum effective channel width for each successive line of transistors.

the total number of pixels in each line which are filled. The devices examined by this process are displayed as devices 'D' and 'E' in figure 5.21. The results of this technique yields the plots shown in figure 5.36. It can be seen that there is a large degree of variation across each channel, with the number of filled pixels varying from an effective channel width of as low as 18.5 μm (3.7% pixels filled) to as high as 45.0 μm (9.0%) in device 'D'. These figures are similar to those for a second high resolution set of images relating to device 'E' from the same sample and serve to emphasise the suitability of applying analysis from one device to many devices in a more general way.

It should be noted that while the maximum values of W_{eff} appear large, these do not affect device behaviour. It is the minimum value of this analysis which provides an upper bound to the true W_{eff}. Furthermore, the maximum value for deivce 'E' is affected by an imaging artefact which appears at the lowermost portion of each image, corresponding to a position in figure 5.36b of ≈18-20 μm.

5.3.6.4 Nanowire Width Distribution

Having analysed several images to understand the nature of the networks of wires it is worth also considering the individual wires themselves. The individual line scans of figure 5.35 can be seen as a collection of individual wires. If each event here is treated as a discrete wire, then some statistics can be collected regarding



(a) Device 'D' **(b)** Device 'E'

Figure 5.37: Plots showing nanowire width distribution for each of transistors 'D' and 'E'.

the number of wires, and their dimensions. A couple of important caveats to bear in mind:

- wires are rarely aligned perpendicularly to image, and so will appear wider than in reality,
- groups of wires may be poorly resolved, indicating a single wide wire in the place of many small wires, and
- wires may appear darker or lighter than then background, depending on their orientation and connectivity, possibly leading to over or under estimates of width.

Having ignored the effect of the above listed problems, a wire width distribution was estimated from each of the two sampling lines of each of the two images considered in detail, and are shown in figures 5.37. A median wire width of 52±10 nm is observed for device 'D', with device 'E' having a median width of 61±12 nm. Range values displayed here are the median absolute deviation.

5.3.6.5 Wire Propagation Algorithm

Having considered various width estimation approaches, it is clear that a way to determine whether a wire forms part of a connected whole is also highly desirable,

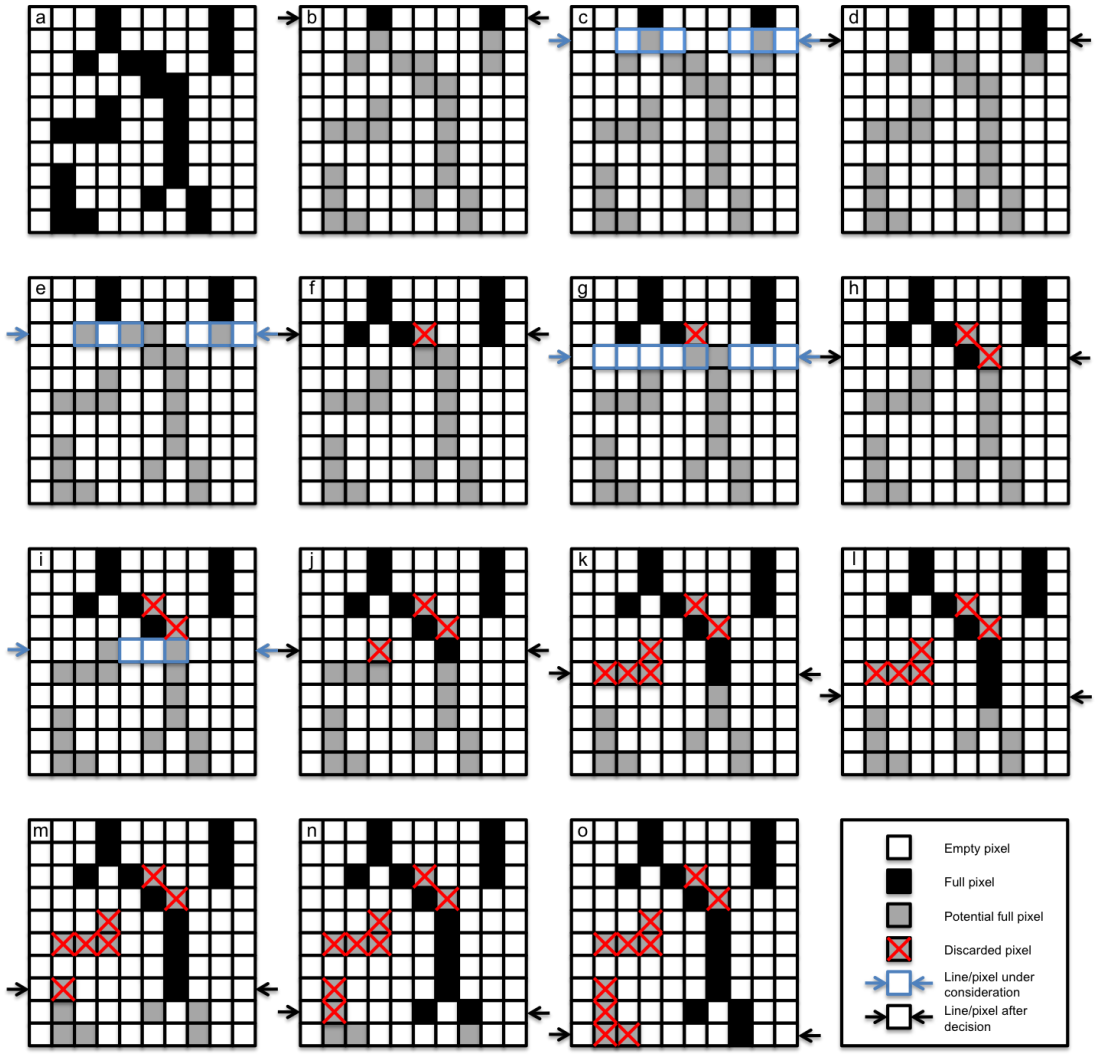


Figure 5.38: Schematic illustration of process to extract only fully connected wires from a binary wire image.

allowing either of of images 2a or 3a from figure 5.34 to be generated from the equivalent image 1a. A further simplification of an image is shown in figure 5.38, which in part a illustrates a sample binary wire mask, and in subsequent steps (b-o) illustrates the process by which a continuous connected wire map may be extracted.

Now we further describe the algorithm illustrated in figure 5.38, allowing it to be automatically implemented:

(a) Select full binary image.

(b) Consider image line 1.

(c) Broaden features of line 1 from step (b) by an amount designed to allow for non-perpendicular wire alignment.

(d) Perform a logical AND of broadened line 1 and line 2.

(e) Repeat process of step (c) with output from step (d).

(f) Perform a logical AND of broadened line 2 and line 3. Note excluded pixel denoted by red cross.

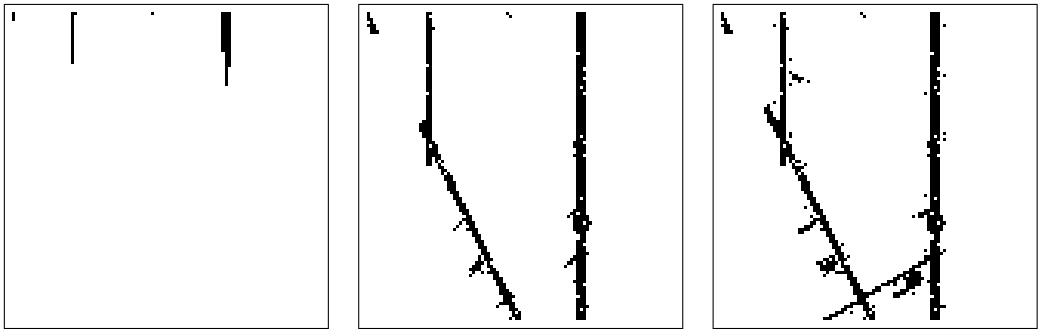
...

(o) Once final line of image is reached, composite function should describe all continuous current paths through image.

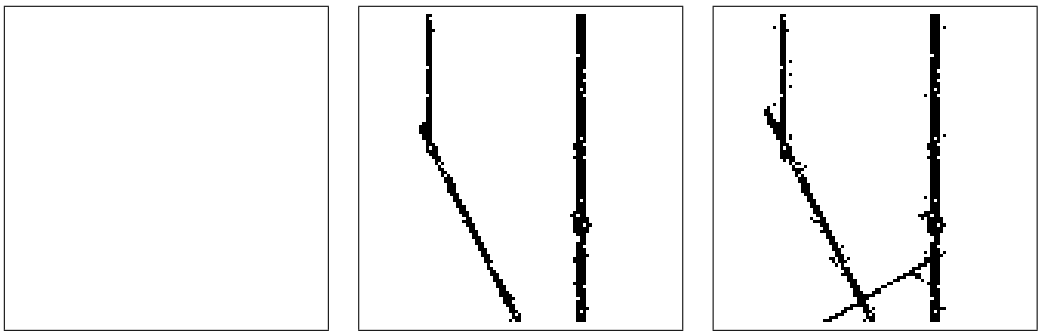
This line detection and connection algorithm was run on a number of binary masks derived from real SEM images, allowing connected wires to be extracted. It will be appreciated that it fails to exclude all branches which do not reach the second contact, such as that which is 'abandoned' by step 'h' in figure 5.38, having begun to propagate from the upper right corner of the grid. However, if the algorithm is first run from top to bottom, and then repeated from bottom to top, it is possible to exclude all such branches from the final mask. As a control input to the algorithm, a broadening term is used. If a value of [1] is used, then only strictly vertical wires will propagate, and any break in the wire or notch will permanently terminate that branch, or segment of width. If a broadening term of [1 1 1] used, then at each line, a pixel either side of the pixel above will be considered. If a broadening term of [1 1 0] is used then the wires will be allowed to propagate to the left but not to the right, and vice versa.

The algorithm described above was implemented in MATLAB, and run on the test image shown in figure 5.39. The image has been generated to approximate a real binary NW SEM image, as generated by image processing steps described earlier (in section 5.3.6.1), and also repeated in figures 5.39 (b) and (c). A number of output images generated by the algorithm are shown, with the width

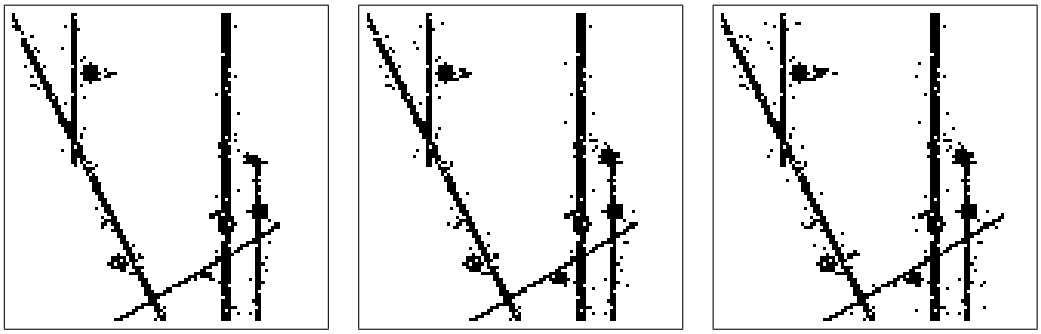
(a) Test image **(b)** Thick wires **(c)** Thin wires



(d) Filter '1': single **(e)** Filter '3': single **(f)** Filter '5': single



(g) Filter '1': dual **(h)** Filter '3': dual **(i)** Filter '5': dual



(j) Filter '7': dual **(k)** Filter '9': dual **(l)** Filter '11': dual

Figure 5.39: Various broadening filters tested for application to wire propagation algorithm.

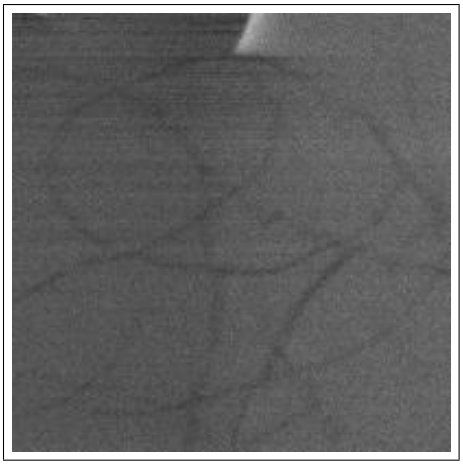
of the dilation filter changed between runs. Figure 5.39d shows the output of the algorithm run with no non-perpendicular alignment (broadening term [1]). The algorithm is then also run in reverse, resulting in a completely blank output, figure 5.39g.

If the propagation requirements are relaxed slightly, and a filter of [1 1 1] is used the resulting image of figure 5.39e is achieved, with the reverse filtered image in figure 5.39h. In the case of the output with a filter of [1 1 1] all vertical wires are retained, as the algorithm can recover from a single missing pixel on any particular line, by broadening the remaining pixels. It can also be seen that wires that are $< 45°$ from perpendicular are preserved, but those that are $> 45°$ are removed from the image. Running the reverse process serves to clean up the image by removing some of the small perturbations left by removed features.

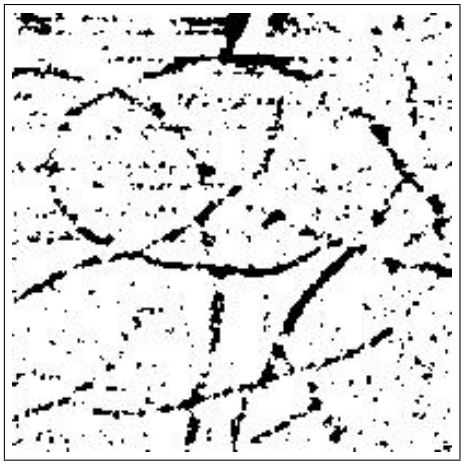
If the filter width is increased to 5 (a filter of [1 1 1 1 1]), as shown in figures 5.39f and 5.39i, features even further from perpendicular are preserved. In this case, the cut-off is $\approx 63°$. Broadening filters of width 7, 9 and 11 are also trialled, with the dual-filtered images shown in figures 5.39j,5.39k and 5.39l respectively.

As the width of filter is increased, more original features are preserved, with features that are unconnected being removed. However, a side effect of increasing the filter width is to allow jumps to be made. If a filter width of 11 is used, then a pixel which is separated by 4 empty pixels can be bridged to. This both serves to enhance the algorithm, by allowing small image anomalies to be removed, but also allows more of the image noise to be retained.

Application of propagation algorithm While trials of this approach suggest that it may be a useful tool, it is not yet considered robust enough to provided a true connected wire extraction tool, primarily due to the challenges associated with binary mask creation. The algorithm described above is weakened by the lack of robust binary images, with the requirement that wires be contiguous not met in many instances. The SEM sub-image of some fine nanowires which has been used previously is now subjected to this algorithm, with the inclusion of a 'dilation' filter before application of the algorithm, to allow some broken wires segments to be re-connected. The inverse, an 'erode' filter is applied as the final step of image processing, to compensate for the wire dilation introduced by this



(a) Original SEM image



(b) Threshold filtered

(c) Dilated

(d) Filter '11': single

(e) Filter '11': dual

(f) Eroded

Figure 5.40: Wire propagation algorithm applied to an SEM image of fine wires, with image dilation and erosion. (SEM image 200x200 pixels, 2.2μm $\times$ 2.2μm.)

step.

Figure 5.40 demonstrates the complete process, and an output image which represents as close an approximation to the number of wires it is felt possible to be measured with this technique, shown in figure 5.40f. It is clear that fine wires are detected, and noise introduced by the initial image processing is to a large extent removed. However, this image is unlikely to provide an accurate representation of the size and connection of wires. Bearing this in mind, it may still be of some value to consider then number of full pixels in the final processed image. In this case 7.0% of the image pixels are filled. However, the highest number of filled pixels in any line is almost 19%, while at least one horizontal line can be drawn on the image without intercepting a single filled pixel. These values indicate the limitations of the approach: a useful qualitative guide can be given, but quantitative analysis remains a challenge.

5.3.7 Effective Channel Estimation and Geometric Correction

Having now estimated the real dimensions of a NW FET it is necessary to apply this information to the parameters extracted from the electrical measurements presented in section 5.3.3.2. While the measurements and estimations made based on image analysis are indicative at best, it is hoped that they can give some guidance as to the true structure and form of NW devices, and help to explain the behaviour observed through electrical measurements.

Table 5.5 provides a summary of extracted device characteristics, with a median mobility extract for NW devices of $1.18\times10^{-3}cm^2/Vs$, with a maximum of as high as $4.0\times10^{-3}cm^2/Vs$. However, if it is considered, as shown in figure 5.36 for example, that the true channel width is in fact closer to 18.5 μm, then that mobility estimate must be increased by a factor of W_{mask}/W_{eff}, in this case 500/18.5, which is ≈ 27. If this was indeed the channel width for all devices the median mobility would be $\approx 32\times10^{-3}cm^2/Vs$, and as high as $108\times10^{-3}cm^2/Vs$.

Furthermore, if such a device was composed of a number of wires with a variety of substrate-wire separations, it has been demonstrated that mobility can easily be under-estimated by a factor of two (for an air-gap of just 50 nm). In addition,

Correction cause	Correction factor	Mobility (cm^2/Vs)	
		Median	Maximum
Initial estimate	-	0.001	0.004
W_{eff}	$\times 27$	0.032	0.108
Capacitance	$\times 2$	0.064	0.217
Continuous path	$\times 2$	0.128	0.433
Indirect path	$\times\sqrt{2}$	0.182	0.613
Cumulative	$\times 153$	0.182	0.613

Table 5.7: Estimation of effective field effect mobility with possible corrections for device geometry.

non-direct wire paths are likely to contribute significantly to the effective channel length. If an average wire angle of 45 ° were used, then a length correction factor of $\sqrt{2}$ would have to be applied to the masked length (L_{mask}).

By disregarding non-connected wires, as demonstrated in section 5.3.6.5, a further correction can be applied to the true channel geometry. If a further factor of two is assumed for this value, then the reported mobility can corrected once more.

Table 5.7 presents some hypothetical mobility values if each of the discussed geometry corrections are applied to NW devices. While it is not suggested that this analysis be adopted, it in intended to demonstrate how a number of significant underestimates can together give a false impression of a device characteristic. In fact, when these limitations are considered it is clear just how significant the error in initial estimated parameter values can be. In some cases, these results suggest that mobility may in fact be as high as $\approx 0.6cm^2/Vs$, which is in close agreement with the highest values published in the literature for single wire field effect mobilities [113], and also close to mobility values reported in the pentacene devices discussed in chapter 4.

5.4 Conclusions

Both n- and p-type OTFTs fabricated from small molecule organic semiconductors were presented on both SiO_2 and SiN_x, demonstrating similar performance to

those commonly reported for similar devices in the literature, providing a useful benchmark against which to assess novel NW devices.

Overall, the low switching voltages and high reproducibility of these NW devices make them a highly realistic candidate for use in applications as switches with the (relatively) high threshold voltages for organic thin film transistors having long been seen as a significant barrier to their adoption as back plane devices to displace amorphous silicon. While further work is needed to understand fully conduction pathways through each device this work shows that, by improving the control over deposition conditions, it is possible to achieve a high level of reliability over an array of devices.

The image analysis work presented explores a number of ideas which can be employed to map the pathways within an individual device. However, efforts were hindered by the initial difficulty in extracting clean high resolution images of individual NWs. If improved input images were available, the line-by-line counting and propagation techniques should be highly effective at describing the network of wires contributing to conduction.

The suggestion that CuPc nanowires permit high efficiency hole transport along the length of wires, as shown by the relative lack of variation with channel length, indicates that high speed devices with power-losses well below those typically seen in OTFTs could be fabricated by this technique, or at least one similar to it.

Chapter 6

Conclusions

This thesis has considered some of the requirements and challenges in the field of organic thin film transistors (OTFTs), in particular in relation to large scale integration using low temperature compatible processes. Processes and materials have been developed, yielding device performance comparable with the state of the art for bottom-contact, bottom-gate organic small molecule organic thin film transistors.

Initially this work explored the controlled deposition of silicon nitride films by PECVD, developing reliable process conditions necessary to produce high quality dielectric films for use in OTFTs at a plastic compatible temperature of 150 °C. Optimal gas flow rates and RF power settings were established, minimising growth rate instability, leakage and surface roughness properties while maximizing electrical breakdown voltage. A variety of films were characterised allowing an investigation into the impact of changes in film composition ([N]/[Si] ratio) on OTFT performance to be studied.

The developed SiN_x films were then applied to OTFT devices, with the effects of dielectric surface treatments investigated. Common practices for SiO_2 based OTFTs were demonstrated to be successful on SiN_x based devices. High performance pentacene OTFTs were fabricated using a bottom-gate bottom-contact structure, initially on a 300 °C SiN_x, before being demonstrated with yet again improved performance on a plastic compatible 150 °C SiN_x. Both mobility enhancements and contact resistance reductions were demonstrated by the application of an optimal surface treatment.

It was also demonstrated that while an N-rich SiN_x is favourable for a-Si:H device fabrication, Si-rich SiN_x tends to perform better with small molecule organic semiconductors, with an average mobility enhancement of approximately 50% over the N-rich alternatives. An improvement of over 30% was seen over devices fabricated on an SiO_2 surface, suggesting that the relatively high Si density at the surface can improve SAM adhesion and resultant surface condition. Si-rich SiN_x also proved to be the most stable of the SiN_x films under bias-stress.

The application of SiN_x films to glass based devices demonstrates the transferability of the process to alternative substrates, and represents a novel combination of device structure and surface treatments. This could lead to an OTFT fabrication strategy which is truly compatible with existing large area electronic fabrication processes. Further, this process could also allow the exploitation of new organic materials as they become available with minimum process modifications.

Limitations with the devices demonstrated are that they do not perform as well as devices with an SiO_2 dielectric in some respects, such as device stability. However, further work in this area is likely to allow the optimisation of surface treatment parameters which may go some way to overcoming such drawbacks.

The development of organic semiconductor nanowire devices was then considered, by exploring the possibilities of combining traditional thin film transistor fabrication techniques with novel organic nanowires and examining the resultant transistor device behaviours. Two-dimensional arrays of nanowire devices were fabricated and analysed, enabling the suitability of devices to large area applications to be assessed.

CuPc nanowire field effect transistors were demonstrated to have mobilities comparable to and often exceeding similar thin film devices, in spite of a necessary corrections to estimated device geometry not being applied. Device operating voltages were a fraction of those seen in thin film devices, suggesting that far smaller fields are required to bring about significant charge accumulation, and suggesting a significantly different, and beneficial, electronic structure can be put to good use by the switch from poly-crystalline films to ultra-long single crystalline nanowires.

It is anticipated that the low temperature, plastic compatible, dielectric de-

veloped in combination with the techniques developed for CuPc nanowires could lead to a discrete gate, large area compatible nanowire device with little further work required.

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